

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

MLB,D1,SCH (Preliminary_Test)

7 / 7 / 12


Page	Contents	Sync	Date
1	Table of Contents	MASTER	
2	System Block Diagram	MASTER	02/15/2011
3	Power Block Diagram	K17 REF	06/30/2009
4	Revision History	MASTER	MASTER
5	BOM Configuration	MASTER	MASTER
6	BOM Configuration	MASTER	MASTER
7	Functional / ICT Test	MASTER	MASTER
8	Power Aliases	MASTER	MASTER
9	Signal Aliases	D1 MLB TEST	01/27/2012
10	CPU DMI/PEG/FDI/RSVD	J30 MLB	07/14/2011
11	CPU CLOCK/MISC/JTAG	J30 MLB	07/14/2011
12	CPU DDR3 INTERFACES	J30 MLB	07/14/2011
13	CPU POWER	J30 MLB	07/14/2011
14	CPU GROUNDS	J30 MLB	07/14/2011
15	CPU DECOUPLING-I	MASTER	MASTER
16	CPU DECOUPLING-II	MASTER	MASTER
17	PCH SATA/PCIE/CLK/LPC/SPI	J13 MLB	09/15/2011
18	PCH DMI/FDI/PM/Graphics	J13 MLB	09/15/2011
19	PCH PCI/USB/TP/RSVD	J13 MLB	09/15/2011
20	PCH GPIO/MISC/NCTF	J13 MLB	09/15/2011
21	PCH POWER	J13 MLB	09/15/2011
22	PCH GROUNDS	J13 MLB	09/15/2011
23	PCH DECOUPLING	J13 MLB	09/15/2011
24	CPU & PCH XDP	J30 MLB	07/14/2011
25	Chipset Support	MASTER	MASTER
26	USB HUB & MUX	J5 AMD	08/17/2011
27	CPU Memory S3 Support	J5 MLB	07/29/2011
28	DDR3 SDRAM Bank A (Rank 0)	J5 MLB	07/14/2011
29	DDR3 SDRAM Bank B (Rank 0)	J5 MLB	07/14/2011
30	DDR3 Termination	MASTER	MASTER
31	DDR3/FRAMEBUF VREF MARGINING	J5 MLB	07/29/2011
32	ALS/CAMERA CONNECTOR	MASTER	MASTER
33	Thunderbolt Host (1 of 2)	J5 MLB KEPLER	11/14/2011
34	Thunderbolt Host (2 of 2)	J5 MLB KEPLER	11/14/2011
35	Thunderbolt Power Support	J5 MLB KEPLER	11/14/2011
36	RIO CONNECTORS	MASTER	MASTER
37	SSD/HDD Connectors	MASTER	MASTER
38	USB 3.0 CONNECTORS	J5 AMD	08/24/2011
39	SMC	D1 SENSORS	02/20/2012
40	SMC Support	D1 SENSORS	02/20/2012
41	LPC+SPI Debug Connector	D1 SENSORS	02/20/2012
42	SMBus Connections	MASTER	MASTER
43	Power Sensor: Load Side	D1 SENSORS	02/20/2012
44	Power Sensor: High Side	D1 SENSORS	02/20/2012
45	Thermal Sensors	D1 SENSORS	02/20/2012

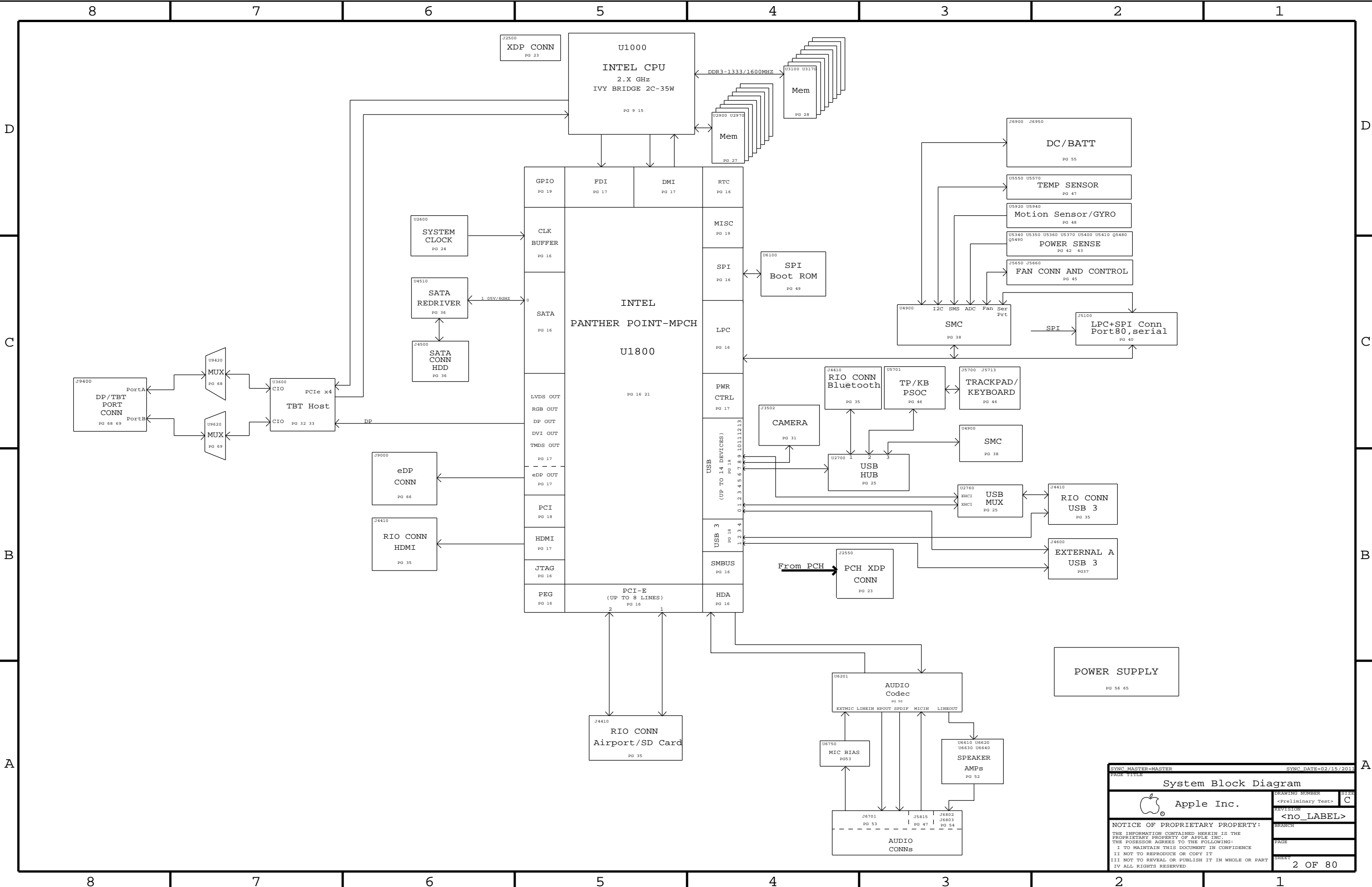
Page	Contents	Sync	Date
46	Fan Connectors	J5 MLB	07/29/2011
47	KEYBOARD/TRACKPAD (1 OF 2)	D2 MLB KEPLER	12/08/2011
48	KEYBOARD/TRACKPAD (2 OF 2)	D2 MLB KEPLER	12/08/2011
49	DIGITAL ACCELEROMETER & GYRO	J5 MLB	07/29/2011
50	SPI ROM	J13 MLB	01/20/2012
51	AUDIO: CODEC/REGULATOR	D1 AUDIO	06/06/2012
52	AUDIO: HEADPHONE FILTER	D1 AUDIO	06/06/2012
53	AUDIO: SPEAKER AMP	D1 AUDIO	06/06/2012
54	AUDIO: JACK	D1 AUDIO	06/06/2012
55	AUDIO: JACK TRANSLATORS	D1 AUDIO	06/06/2012
56	DC-In & Battery Connectors	MASTER	MASTER
57	PBus Supply & Battery Charger	MASTER	MASTER
58	System Agent Supply	MASTER	MASTER
59	5V / 3.3V Power Supply	MASTER	MASTER
60	1.5V DDR3 Supply	MASTER	MASTER
61	CPU IMVP7 & AXG VCore Regulator	MASTER	MASTER
62	CPU IMVP7 & AXG VCore Output	MASTER	MASTER
63	CPUVCCIO (1.05V) Power Supply	MASTER	MASTER
64	Misc Power Supplies	MASTER	MASTER
65	Power FETs	MASTER	MASTER
66	Power Control 1/ENABLE	MASTER	MASTER
67	eDP Display Connector	D1 SENSORS	07/11/2012
68	DDC Crossbar	MASTER	MASTER
69	Thunderbolt Connector A	J5 MLB KEPLER	11/14/2011
70	Thunderbolt Connector B	J5 MLB KEPLER	11/14/2011
71	LCD Backlight Driver (LP8545)	J5 MLB KEPLER	09/21/2011
72	CPU Constraints	J5 MLB	09/13/2011
73	Memory Constraints	J5 MLB	09/13/2011
74	PCH Constraints 1	J5 MLB KEPLER	09/21/2011
75	PCH Constraints 2	J5 MLB	07/29/2011
76	Thunderbolt Constraints	T20 CR	08/31/2011
77	SMC Constraints	J5 MLB	07/29/2011
78	Project Specific Constraints	J5 MLB	07/29/2011
79	PCB Rule Definitions	J5 MLB	07/29/2011
80	Power Sensors: Extended	D1 SENSORS	07/11/2012

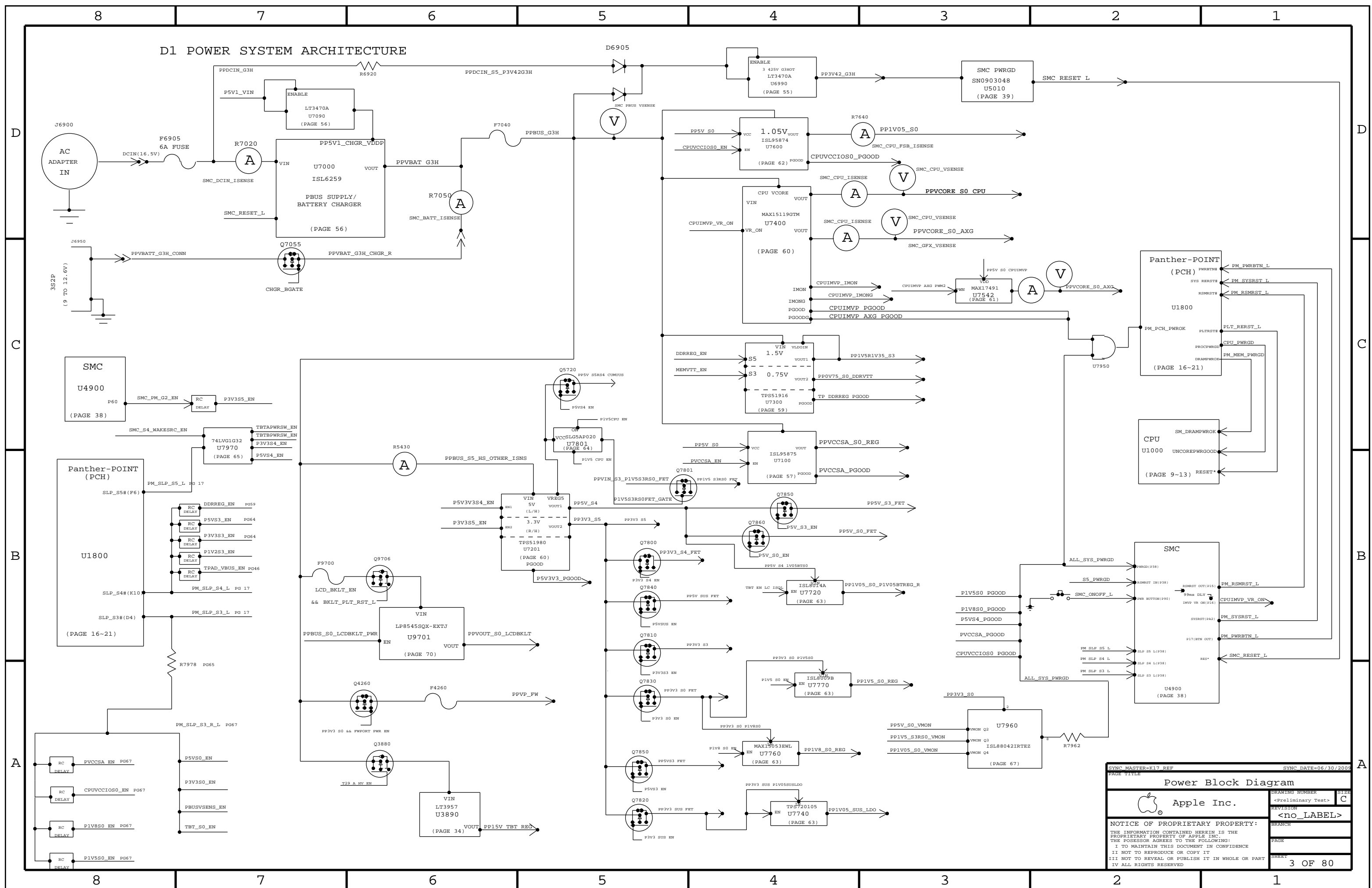
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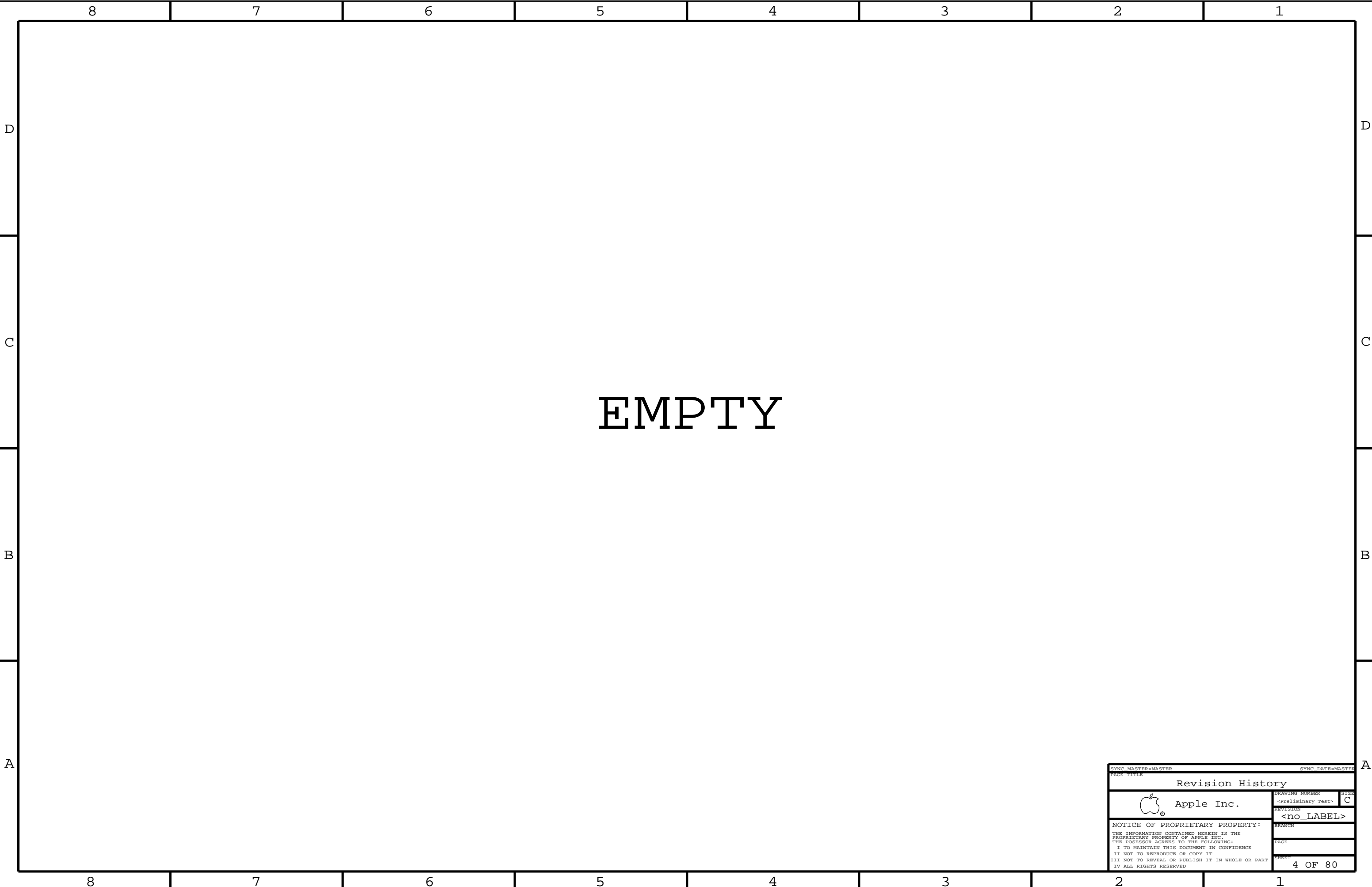
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Preliminary_Test	1	SCHEM MLB D1	SCH	CRITICAL	
820-3190	1	PCBF MLB(NEW 2) D1	PCB	CRITICAL	


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DRAWING NUMBER	SIZE																
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BRANCH																	
PAGE																	
SHEET																	
1 OF 80																	
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Revision History		DRAWING NUMBER	SIZE
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		BRANCH	
		PAGE	
		SHEET	4 OF 80

BOM Variants

[illegible]

Bar Code Labels / EEE #'s

[illegible]

Module Parts

[illegible]

D1 BOM GROUPS

[illegible]

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

Alternate Parts


[illegible]

Alternate Parts

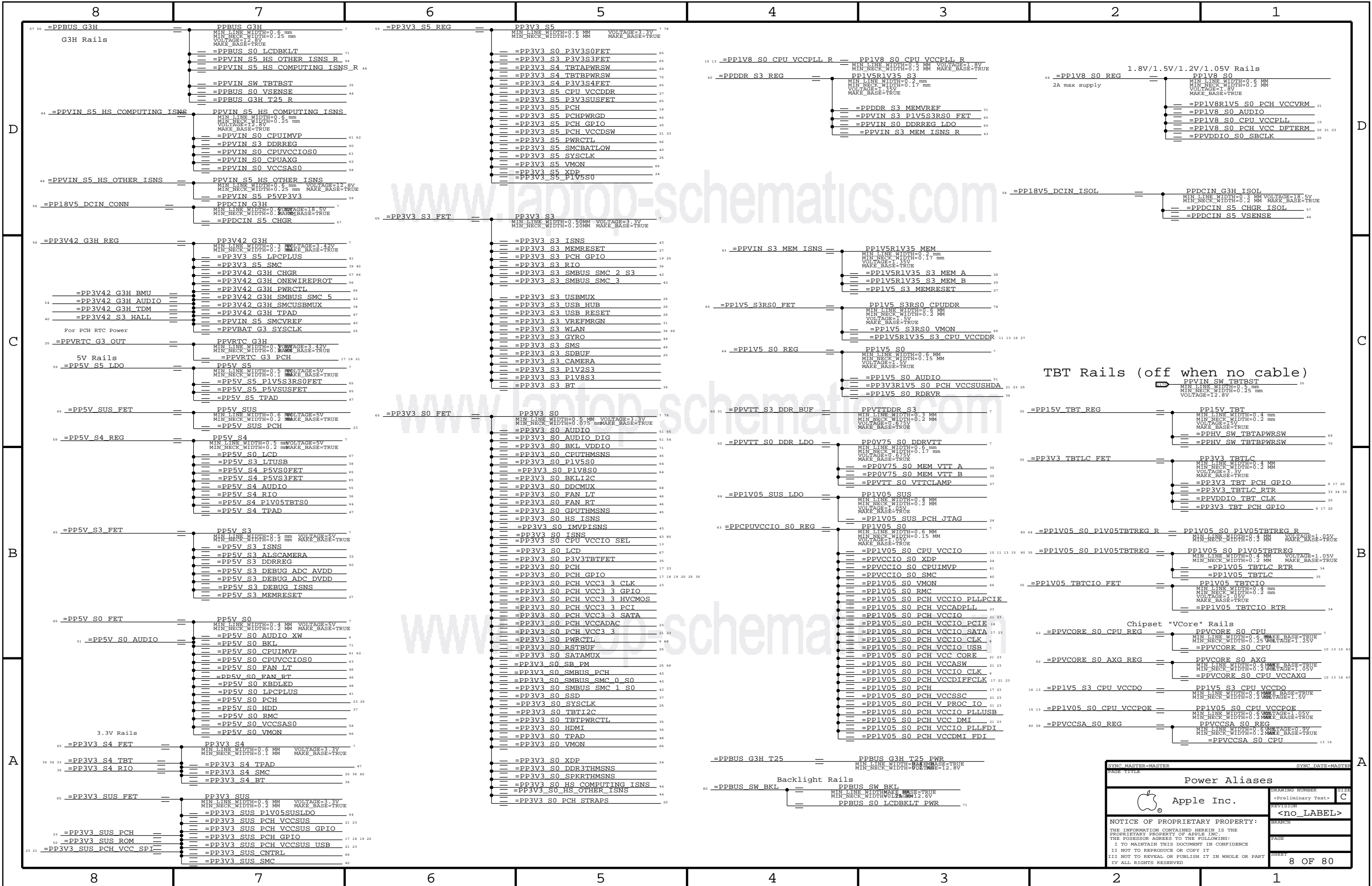
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		SHEET	6 OF 80

8	7	6	5	4	3	2	1
Functional Test Points		POWER RAILS		ICT Test Points		S2 CAMERA PCIE SIGNALS	
J5650 (LEFT FAN CONN)		J5713 (KEY BOARD CONN)		CPU NO_TESTS		NC PCIE CAMERA D2RP	
FANC_TEST PP5V S0		PP3V3 S4		TP TBT MONDC0		PCIE EXCARD D2R N	
FAN LT PWM		WS KBD1		TP TBT MONDC1		PCIE EXCARD D2R P	
FAN LT TACH		WS KBD2		TP TBT PCIE RESET0 L		PCIE EXCARD R2D CN	
J5660 (RIGHT FAN CONN)		WS KBD3		TP TBT PCIE RESET1 L		PCIE EXCARD R2D C N	
FAN RT PWM		WS KBD4		TP TBT PCIE RESET2 L		PCIE EXCARD R2D C P	
FAN RT TACH		WS KBD5		TP TBT PCIE RESET3 L		PCIE CLK100M CAMERAN	
GND		WS KBD6		TP TBT PCIE RESET4 L		PCIE CLK100M CAMERAP	
J3502 (ALS/CAMERA CONN)		WS KBD7		TP TBT XTAL25OUT		PCIE CLK100M EXCARD N	
SMBUS_SMC_2_S3_SDA		WS KBD8		TP DP TBTSRC ML CP<3>		PCIE CLK100M EXCARD P	
SMBUS_SMC_2_S3_SCL		WS KBD9		TP DP TBTSRC ML CN<3>		PCIE ENET R2D C P	
PP5V S3 ALS/CAMERA F		WS KBD10		TP DP TBTSRC ML CN<2>		PCIE ENET R2D C N	
J4400 (RIO CABLE CONN)		WS KBD11		TP DP TBTSRC ML CN<1>		PCIE AP R2D C P	
PP3V3 S4		WS KBD12		TP DP TBTSRC ML CP<2>		PCIE AP R2D C N	
PP3V3 S3		WS KBD13		TP DP TBTSRC ML CN<2>		PCIE AP D2R P	
PP3V3 WLAN F		WS KBD14		TP DP TBTSRC ML CP<1>		PCIE AP D2R PI P	
PP5V S4		WS KBD15 CAP		TP DP TBTSRC ML CN<1>		PCIE AP D2R PI N	
PP1V5 S0		WS KBD16 NUM		TP DP TBTSRC ML CP<0>		PCIE AP R2D PI P	
J4410 (RIO FLEX CONN)		WS KBD17		TP DP TBTSRC ML CN<0>		PCIE AP R2D PI N	
USB EXT0 OC L		WS KBD18		TP DP TBTSRC AUXCH CP		PCIE AP R2D PI N	
HDMI IG DDC CLK		WS KBD19		TP DP TBTSRC AUXCH CN		PCIE CLK100M PCH P	
HDMI IG DDC DATA		WS KBD20		TP SPI CS1 L		PCIE CLK100M PCH N	
HDMI HPD L		WS KBD21		TP PCH GPIO8		PCIE CLK100M TBT P TRUE	
PM SLP S3 L		WS KBD22		TP PCH STRP BBS1		PCIE CLK100M TBT N	
PM SLP S4 L		WS KBD23		TP PCH STRP ESI L		PCIE CLK100M SSD P	
AP CLKREQ O L		WS KBD24		TP PCH TP23		PCIE CLK100M SSD N	
ENET RESET L		WS KBD25		TP PCI CLK33M OUT2		PCIE CLK100M SSD N	
ENET CLKREQ L		WS KBD26		TP PCIE CLK100M PEGAN		PCIE CLK100M SSD N	
SD PWR EN		WS KBD27		TP PCIE CLK100M PEGAP		PCIE CLK100M SSD N	
SDCONN STATE CHANGE_SMC		WS KBD28		TP PM SLP A L		PCIE CLK100M SSD N	
PCIE WAKE L		WS KBD29		TP PVOUT PCH DCPUSUBYP		PCIE CLK100M SSD N	
AP CLKREQ O L		WS KBD30		TP SMC MPMS LED PWR		PCIE CLK100M SSD N	
AP RESET CONN L		WS KBD31		TP SMC MPMS LED CHG		PCIE CLK100M SSD N	
WIFI EVENT L		WS KBD32		TP SMS INT2		PCIE CLK100M SSD N	
USB EXT0 P		WS KBD33		PCIE TBT R2D C P<3..0>		PCIE CLK100M SSD N	
USB BT CONN P		WS KBD34		PCIE TBT R2D C N<3..0>		PCIE CLK100M SSD N	
USB BT CONN N		WS KBD35		PCIE TBT R2D C P<3..0>		PCIE CLK100M SSD N	
AP RESET CONN L		WS KBD36		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMBUS_PCH_CLK		WS KBD37		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMBUS_PCH_DATA		WS KBD38		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMBUS_SMC_1_S0_SCL		WS KBD39		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMBUS_SMC_1_S0_SDA		WS KBD40		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
J5815 (KBD BACKLIGHT CONN)		WS KBD41		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
PP_KBD_BOOST_VOUT		WS KBD42		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
KBDLED_CATHODE1		WS KBD43		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
KBDLED_CATHODE2		WS KBD44		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMC_KBDLED_PRESENT L		WS KBD45		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
J6950 (MAIN BATT CONN)		WS KBD46		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
PPVBAT G3H CONN		WS KBD47		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMBUS_SMC_5_G3_SCL		WS KBD48		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMBUS_SMC_5_G3_SDA		WS KBD49		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SYS_DETECT L R		WS KBD50		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SYSDET1		WS KBD51		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SYSDET 3 4		WS KBD52		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
J6801 (2 MIC CONN)		WS KBD53		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
CON_DMIC_PWR		WS KBD54		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
CON_DMIC_SDA1		WS KBD55		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
CON_DMIC_CLK		WS KBD56		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
J3401 & J3402 (AIRPORT/BT/CAMERA CONN)		WS KBD57		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
PCIE_CLK100M_AP_CONN_P		WS KBD58		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
PCIE_CLK100M_AP_CONN_N		WS KBD59		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
AP_CLKREQ O L		WS KBD60		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
AP_RESET CONN L		WS KBD61		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
PP5V S3 WLAN F		WS KBD62		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
PP5V S3 ALS/CAMERA F		WS KBD63		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
SMBUS_SMC_2_S3_SDA		WS KBD64		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
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USB_CAMERA_CONN_P		WS KBD66		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	
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GND		WS KBD93		PCIE TBT R2D C P<3..1>		PCIE CLK100M SSD N	




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PAGE TITLE

Power Aliases



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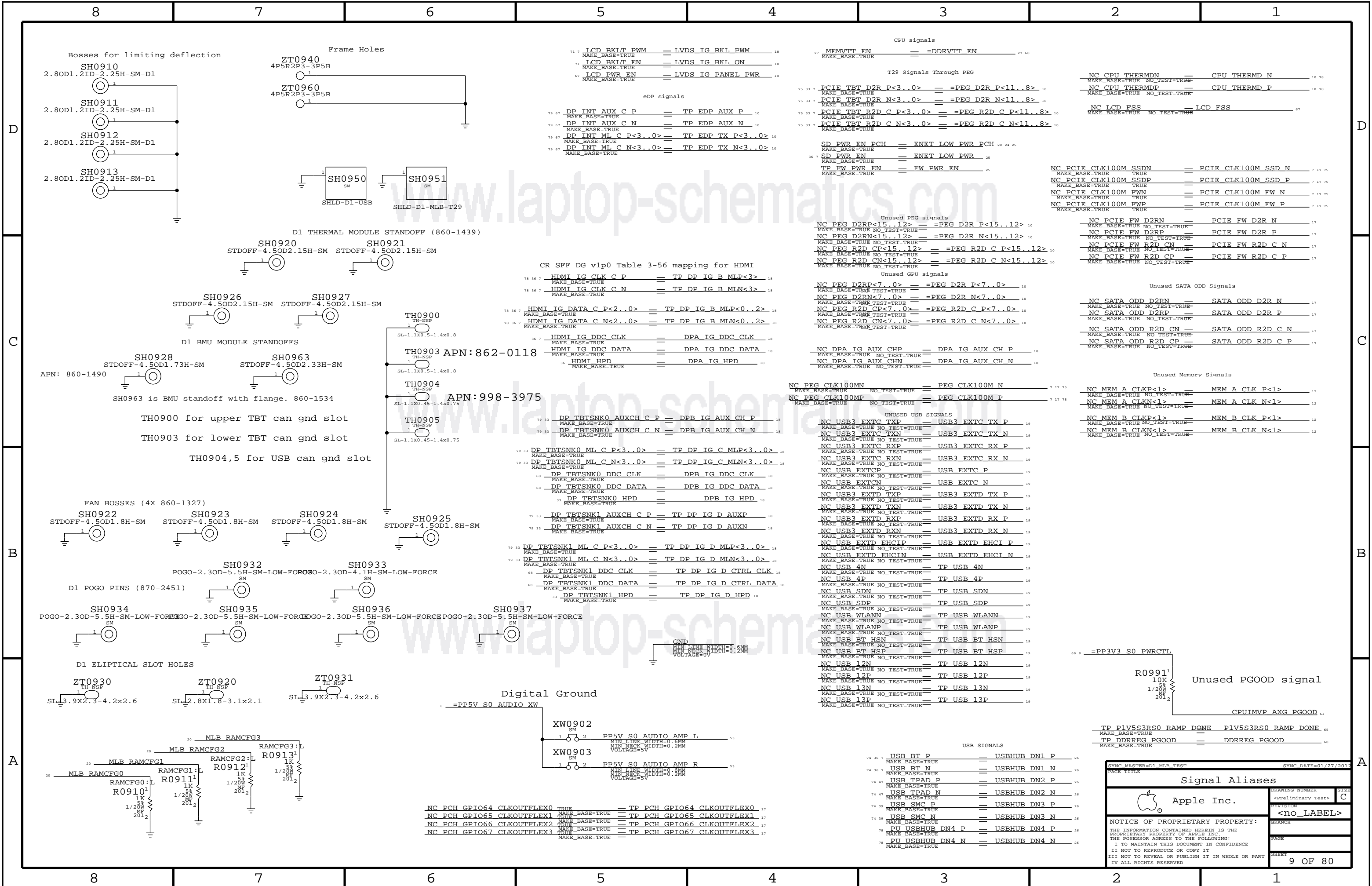
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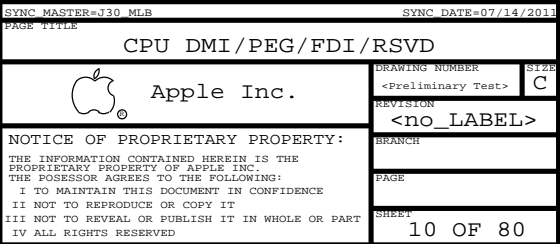
8 OF 80

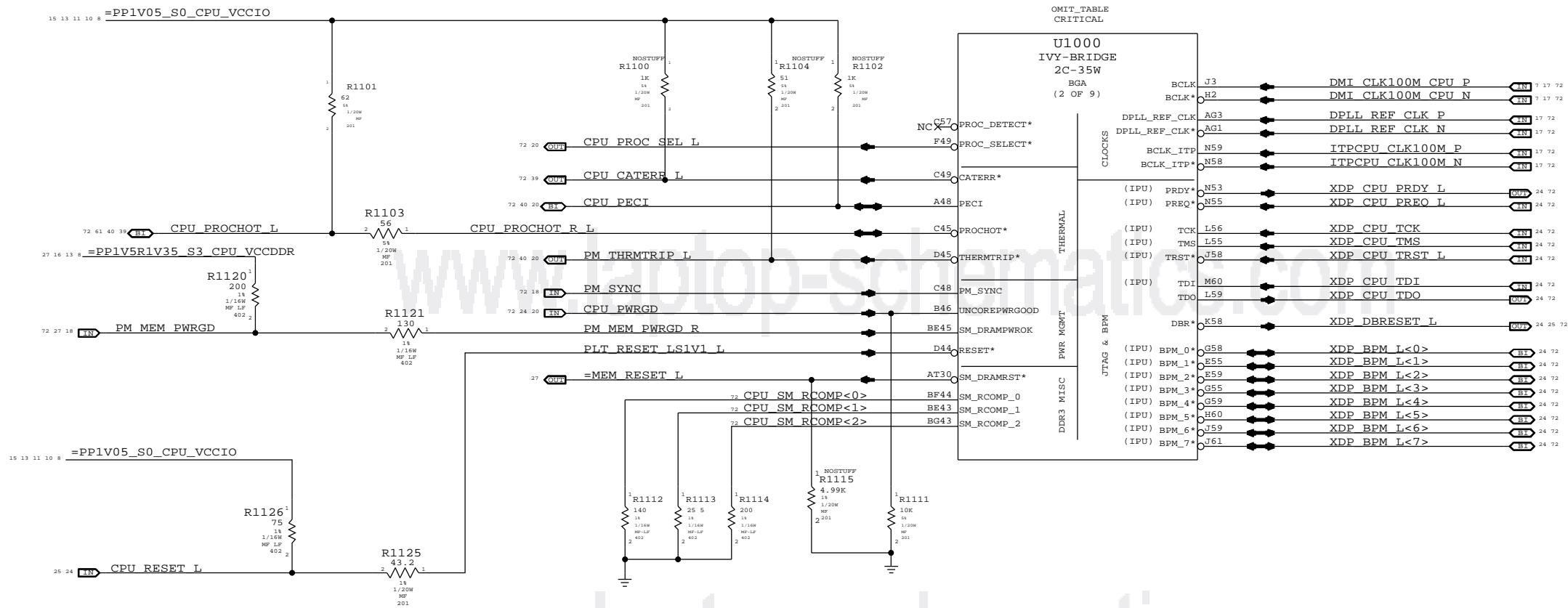
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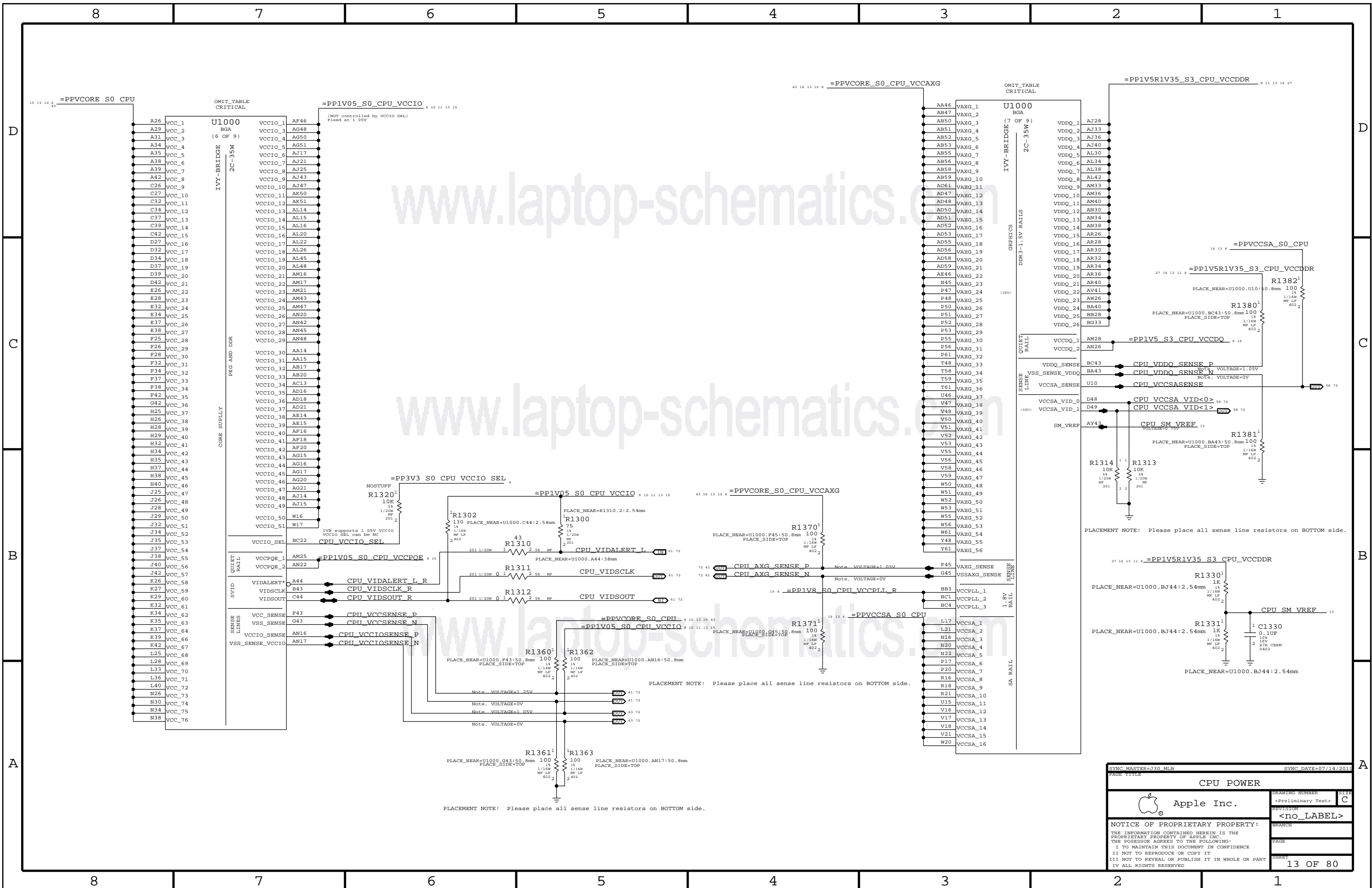


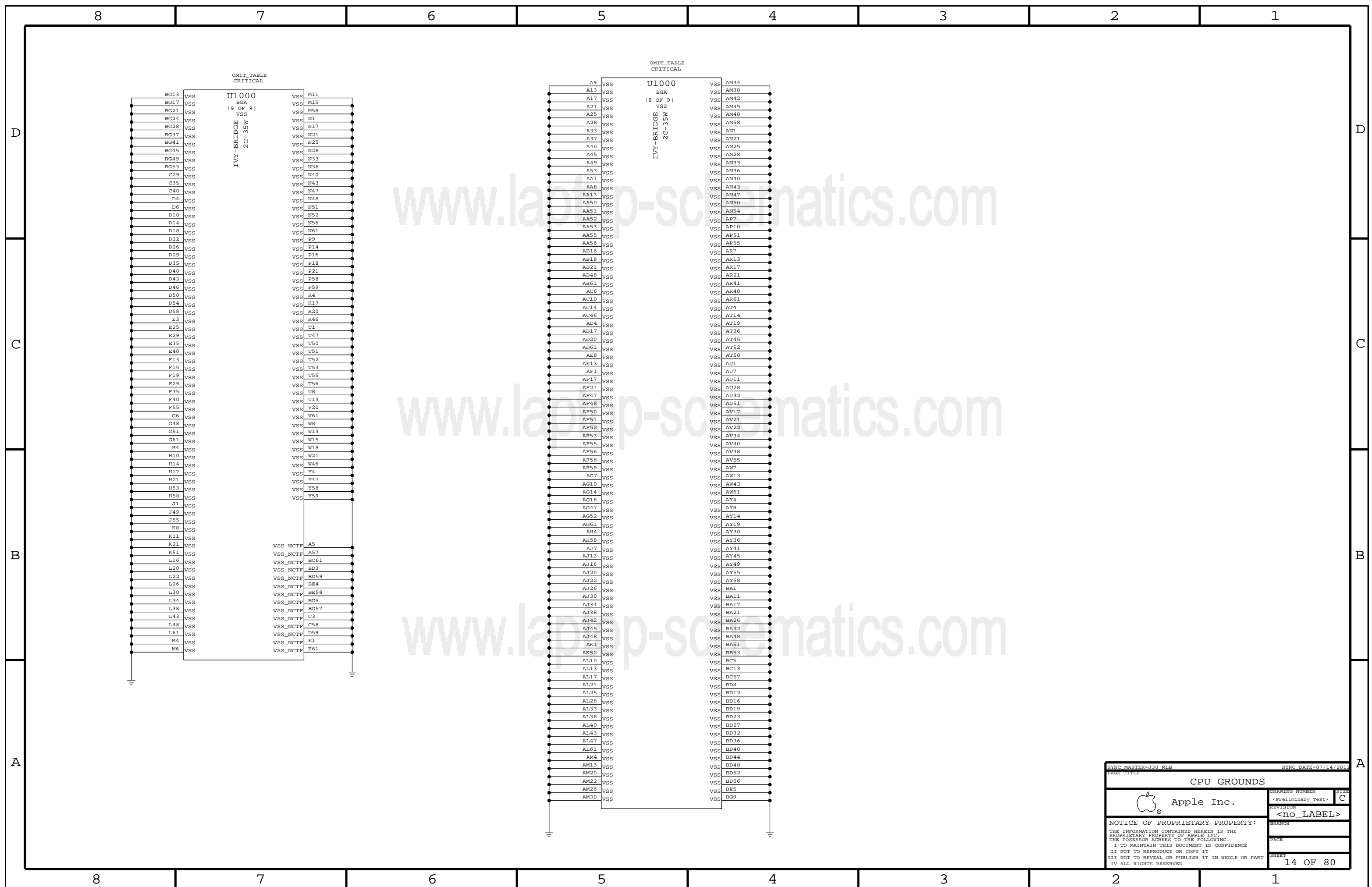
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				9 OF 80	











Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF

Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF



Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

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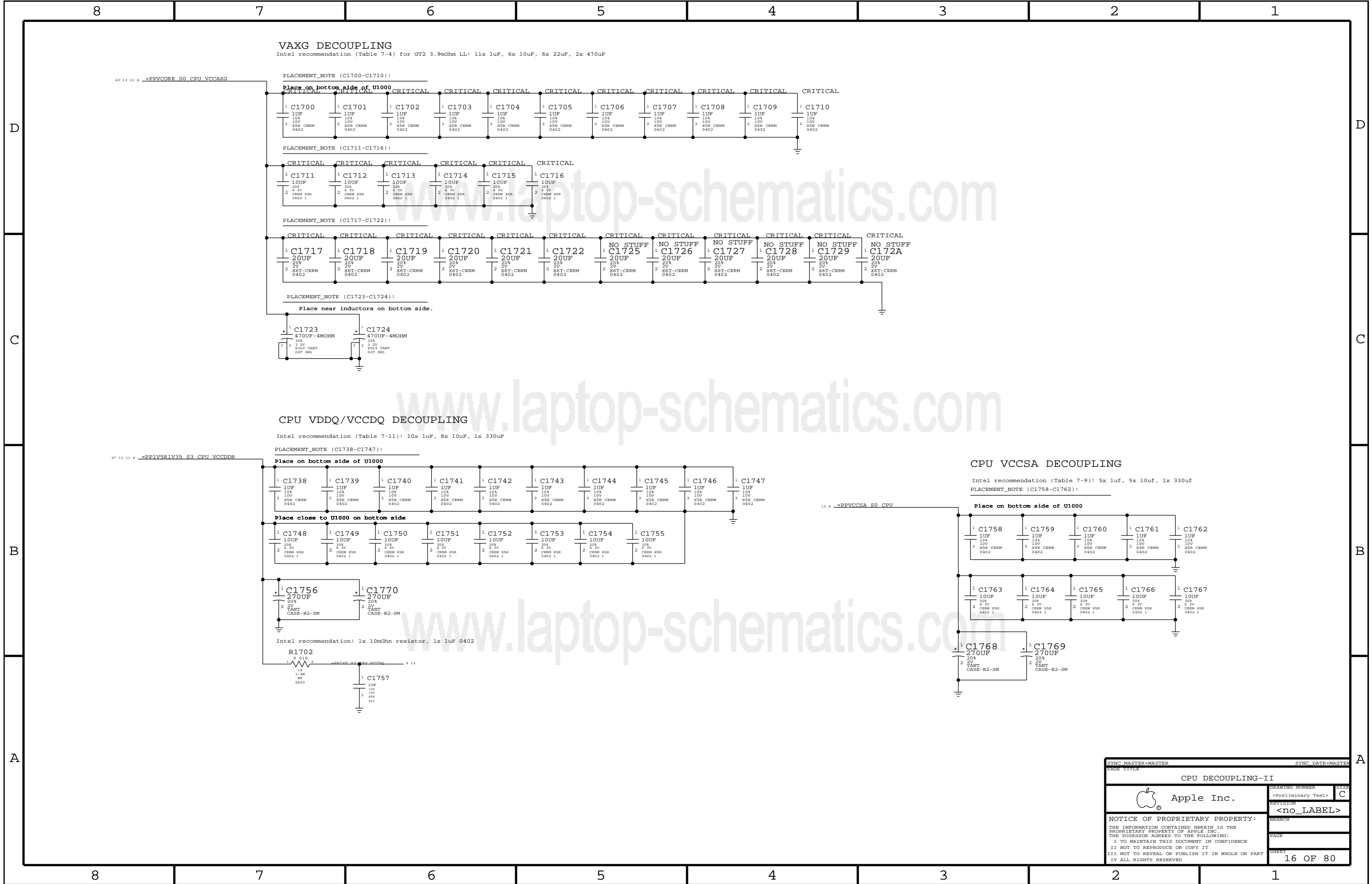


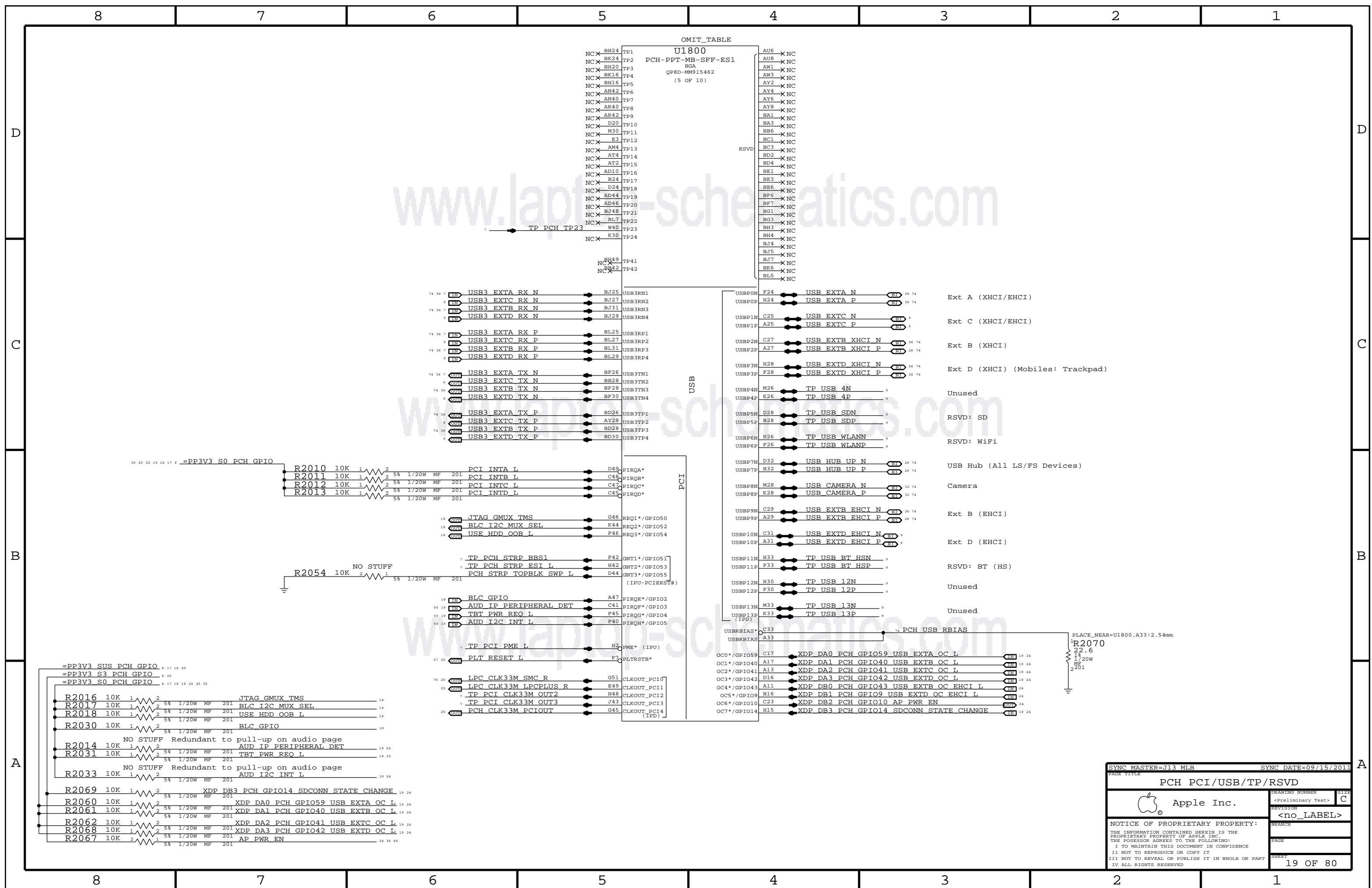
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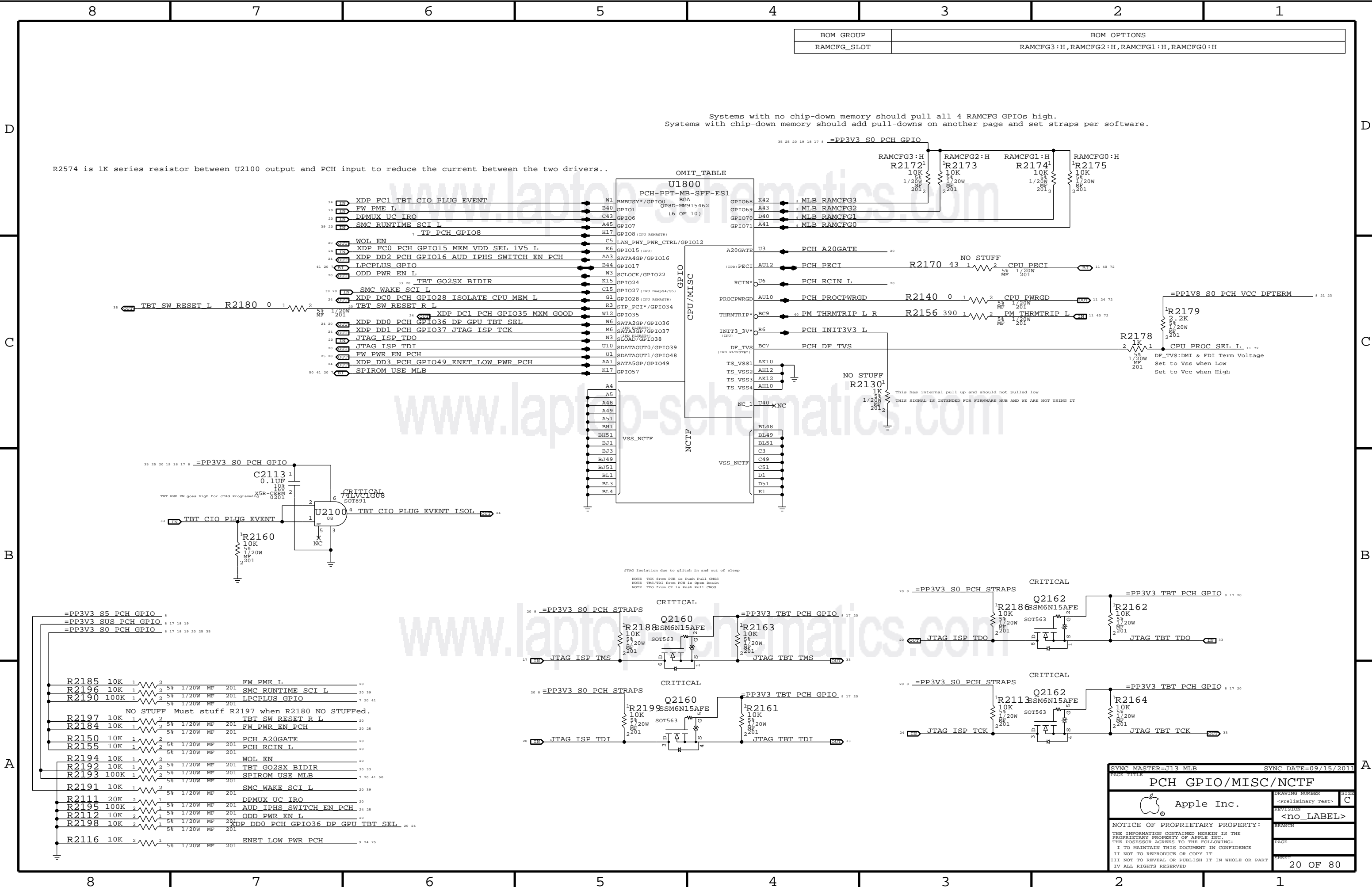
Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

A







BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

R2574 is 1K series resistor between U2100 output and PCH input to reduce the current between the two drivers..

OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
GPIO0 BGA
GPIO1 QP8D-MM915462
(6 OF 10)

24	GPIO0	W1	XDP FC1 TBT CIO PLUG EVENT
20	GPIO1	B40	FW PME L
20	GPIO6	C43	DEMUX UC IRO
39	GPIO7	A45	SMC RUNTIME SCI L
7	GPIO8	H17	TP PCH GPIO8
20	GPIO15	C5	WOL EN
24	GPIO16	K6	XDP FC0 PCH GPIO15 MEM VDD SEL 1V5 L
24	GPIO16	AA3	XDP DD2 PCH GPIO16 AUD IPHS SWITCH EN PCH
41	GPIO17	B44	LPCPLUS GPIO
20	GPIO17	W3	ODD PWR EN L
33	GPIO28	K15	TBT GO2SX BIDIR
39	GPIO28	C15	SMC WAKE SCI L
20	GPIO28	G1	XDP DC0 PCH GPIO28 ISOLATE CPU MEM L
24	GPIO35	R3	TBT SW RESET R L
24	GPIO36	W12	XDP DC1 PCH GPIO35 MXM GOOD
24	GPIO37	W6	XDP DD0 PCH GPIO36 DP GPU TBT SEL
24	GPIO37	M6	XDP DD1 PCH GPIO37 JTAG ISP TCK
20	GPIO38	N3	JTAG ISP TDO
20	GPIO39	U10	JTAG ISP TDI
25	GPIO49	U1	FW PWR EN PCH
24	GPIO49	AA1	XDP DD3 PCH GPIO49 ENET LOW PWR PCH
50	GPIO57	K17	SPIROM USE MLB

A4	GPIO57	K17	SPIROM USE MLB
A5	GPIO57	K17	SPIROM USE MLB
A48	GPIO57	K17	SPIROM USE MLB
A49	GPIO57	K17	SPIROM USE MLB
A51	GPIO57	K17	SPIROM USE MLB
BH1	GPIO57	K17	SPIROM USE MLB
BH51	GPIO57	K17	SPIROM USE MLB
BJ1	GPIO57	K17	SPIROM USE MLB
BJ3	GPIO57	K17	SPIROM USE MLB
BJ49	GPIO57	K17	SPIROM USE MLB
BJ51	GPIO57	K17	SPIROM USE MLB
BL1	GPIO57	K17	SPIROM USE MLB
BL3	GPIO57	K17	SPIROM USE MLB
BL4	GPIO57	K17	SPIROM USE MLB

GPIO68	A42	MLB RAMCFG3
GPIO69	A43	MLB RAMCFG2
GPIO70	D40	MLB RAMCFG1
GPIO71	A41	MLB RAMCFG0

A20GATE	U3	PCH A20GATE
PECI	AU12	PCH Peci
RCIN	U6	PCH RCIN L
PROCPWRGD	AU10	PCH PROCPWRGD
THRMTRIP	BC9	PM THRMTRIP L R
INIT3_3V	R6	PCH INIT3V3 L
DF_TVS	BC7	PCH DF TVS

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INIT3_3V	R6	PCH INIT3V3 L
DF_TVS	BC7	PCH DF TVS

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
RAMCFG0:H	R2175	10K	1/20W	MF	201

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
RAMCFG0:H	R2175	10K	1/20W	MF	201

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
RAMCFG0:H	R2175	10K	1/20W	MF	201

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
RAMCFG0:H	R2175	10K	1/20W	MF	201

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
RAMCFG0:H	R2175	10K	1/20W	MF	201

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
RAMCFG0:H	R2175	10K	1/20W	MF	201

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
RAMCFG0:H	R2175	10K	1/20W	MF	201

RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
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RAMCFG0:H	R2175	10K	1/20W	MF	201

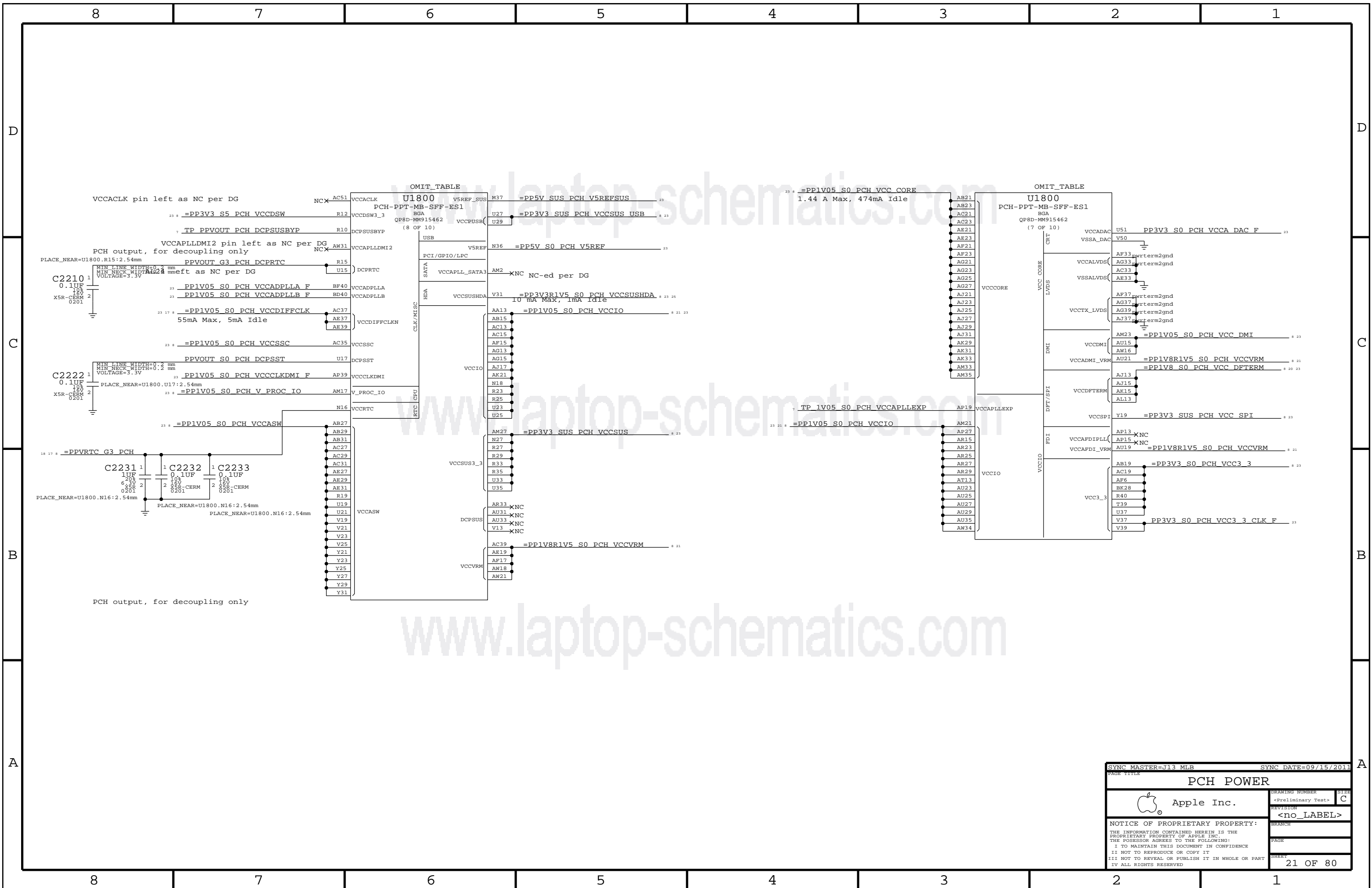
RAMCFG3:H	R2172	10K	1/20W	MF	201
RAMCFG2:H	R2173	10K	1/20W	MF	201
RAMCFG1:H	R2174	10K	1/20W	MF	201
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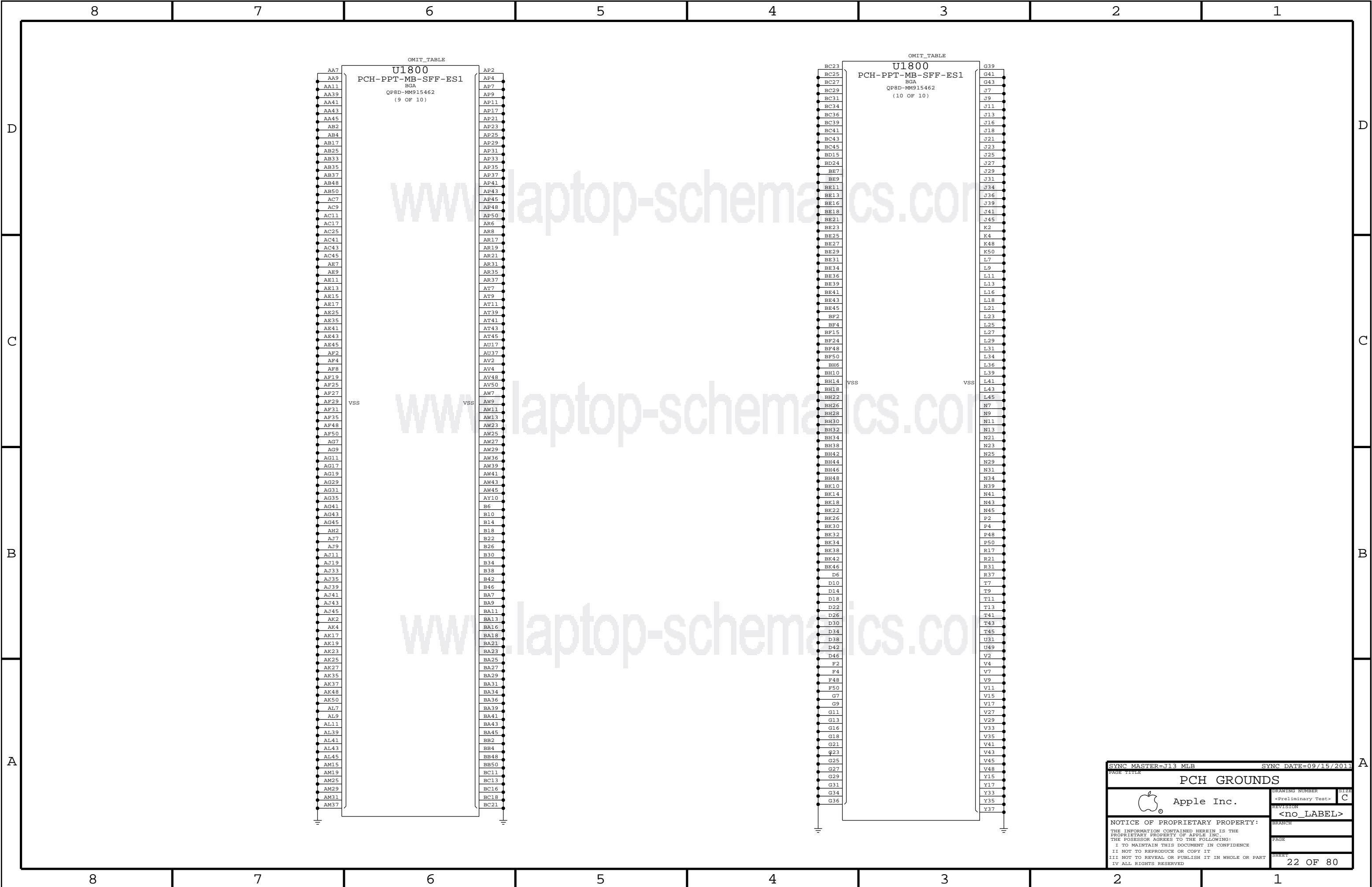
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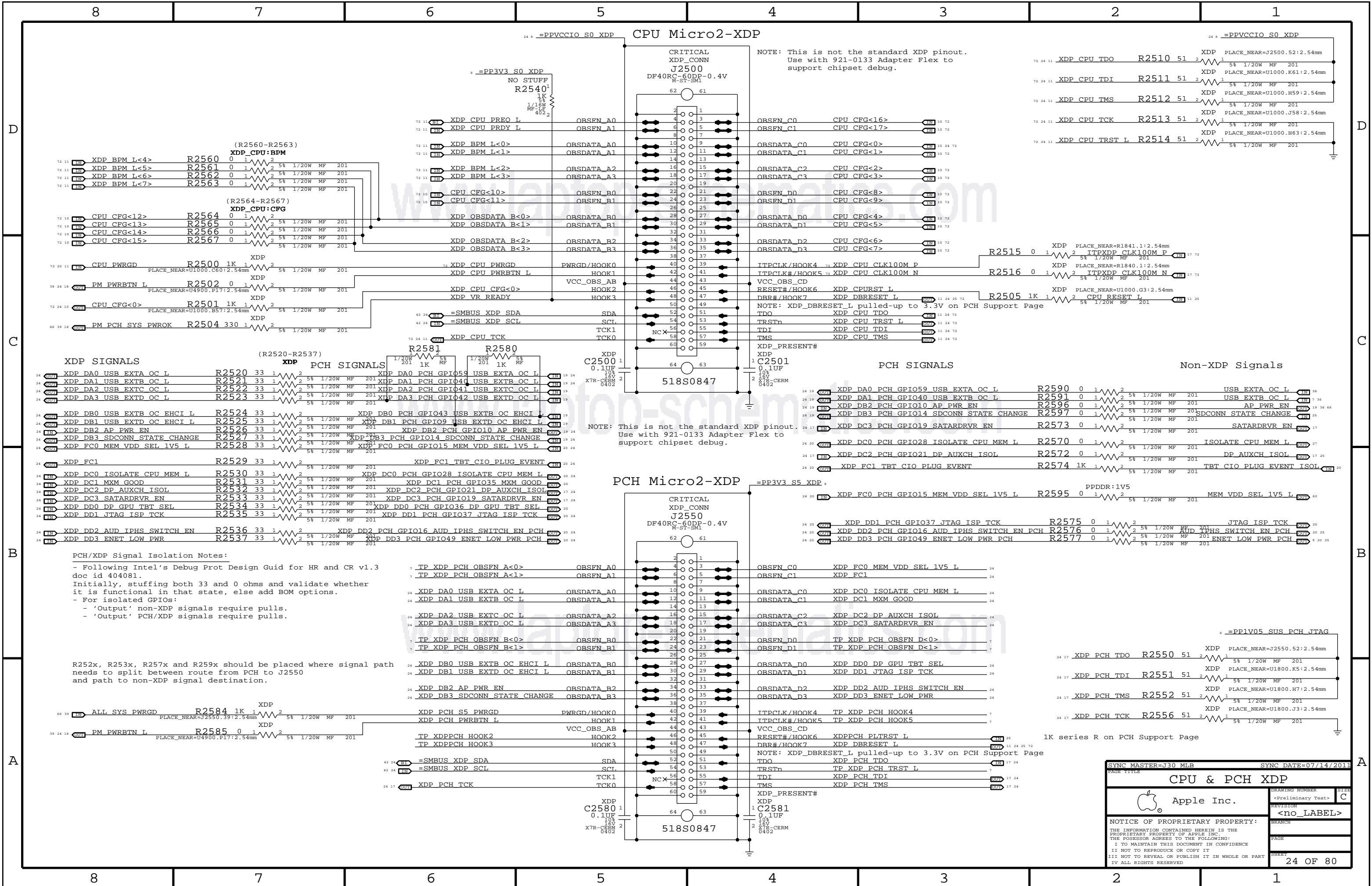
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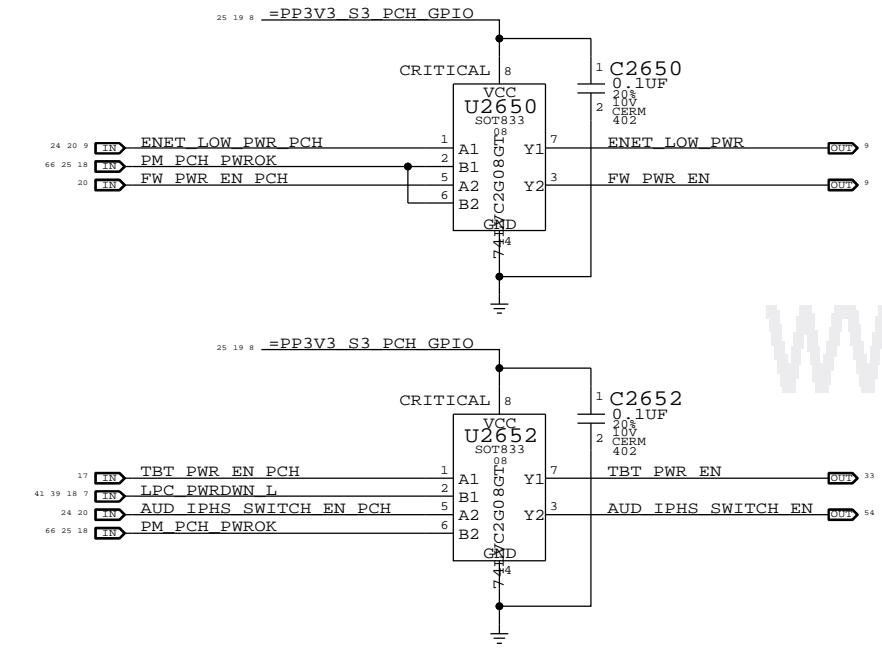
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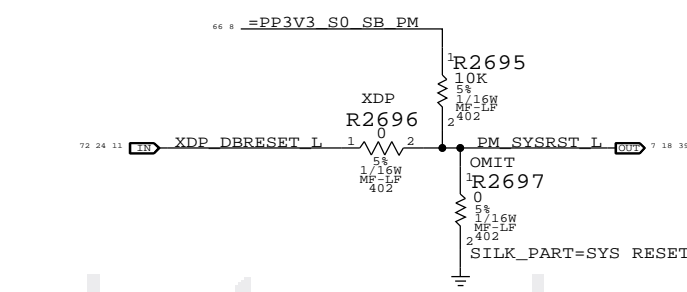
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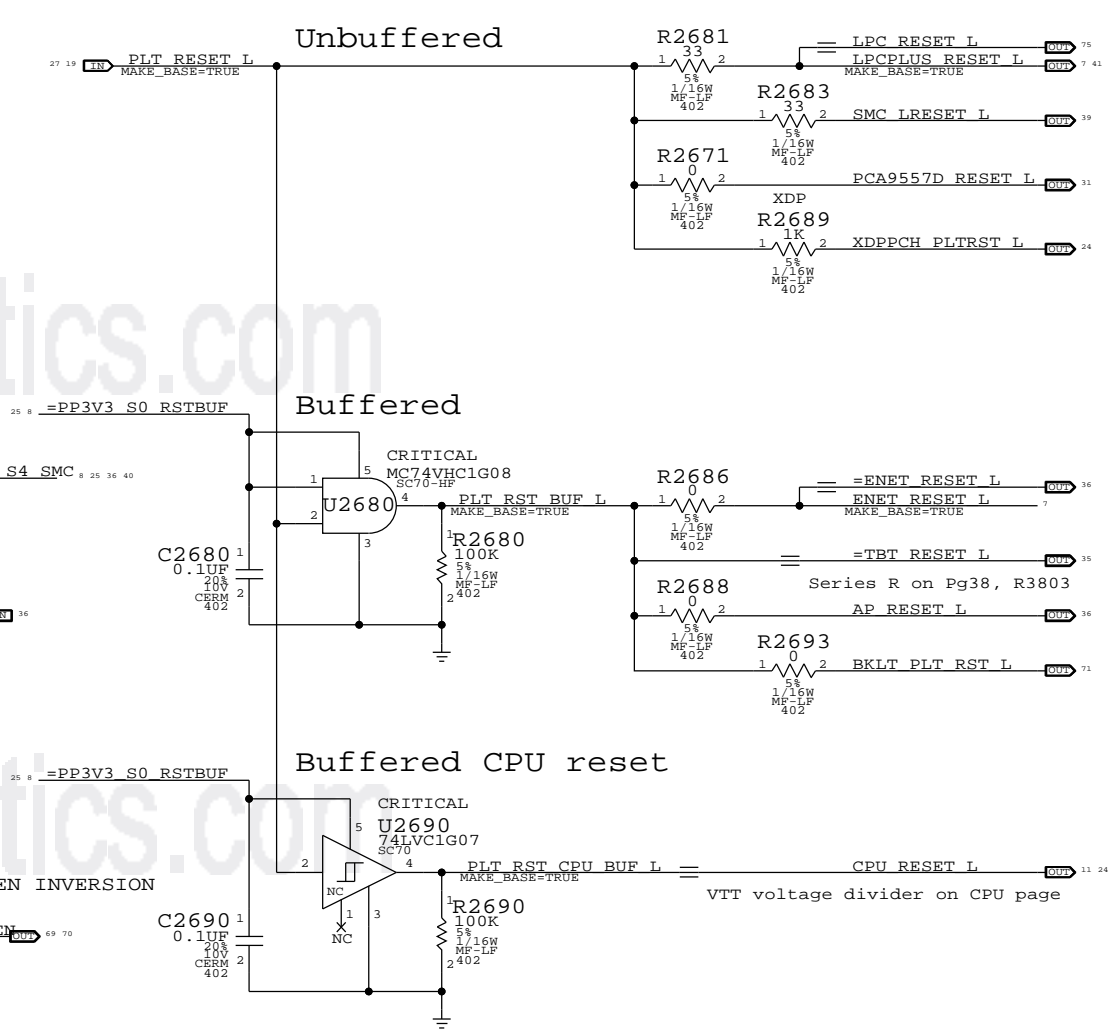
GPIO Glitch Prevention



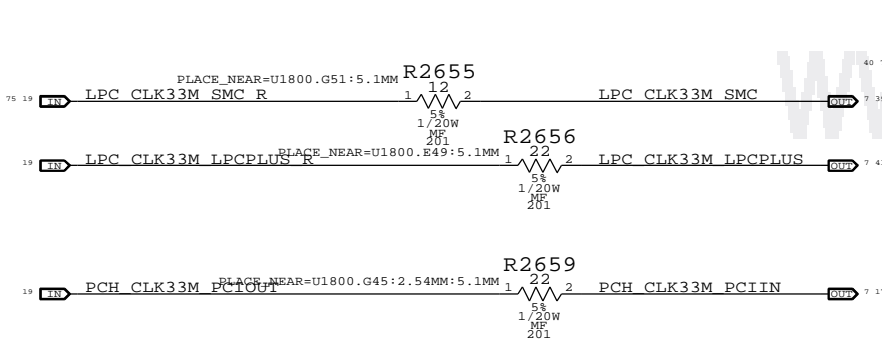
PCH Reset Button



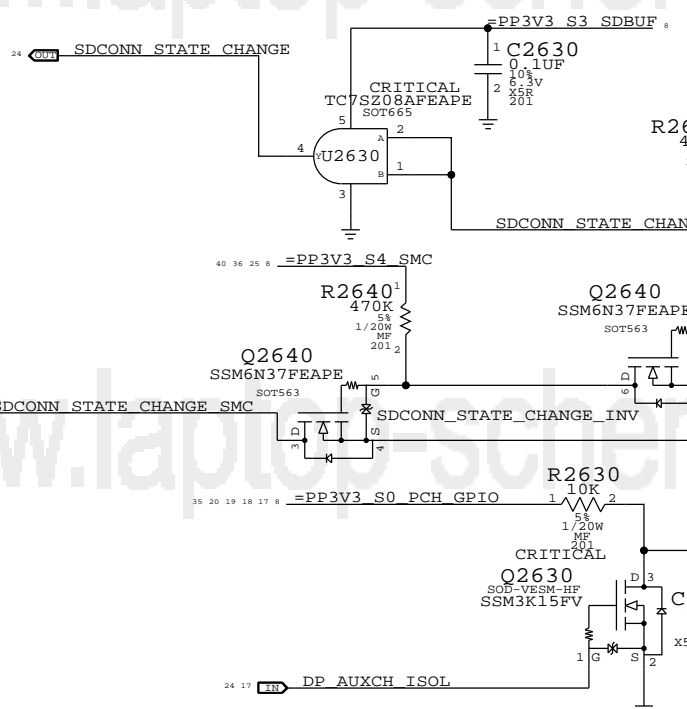
Platform Reset Connections



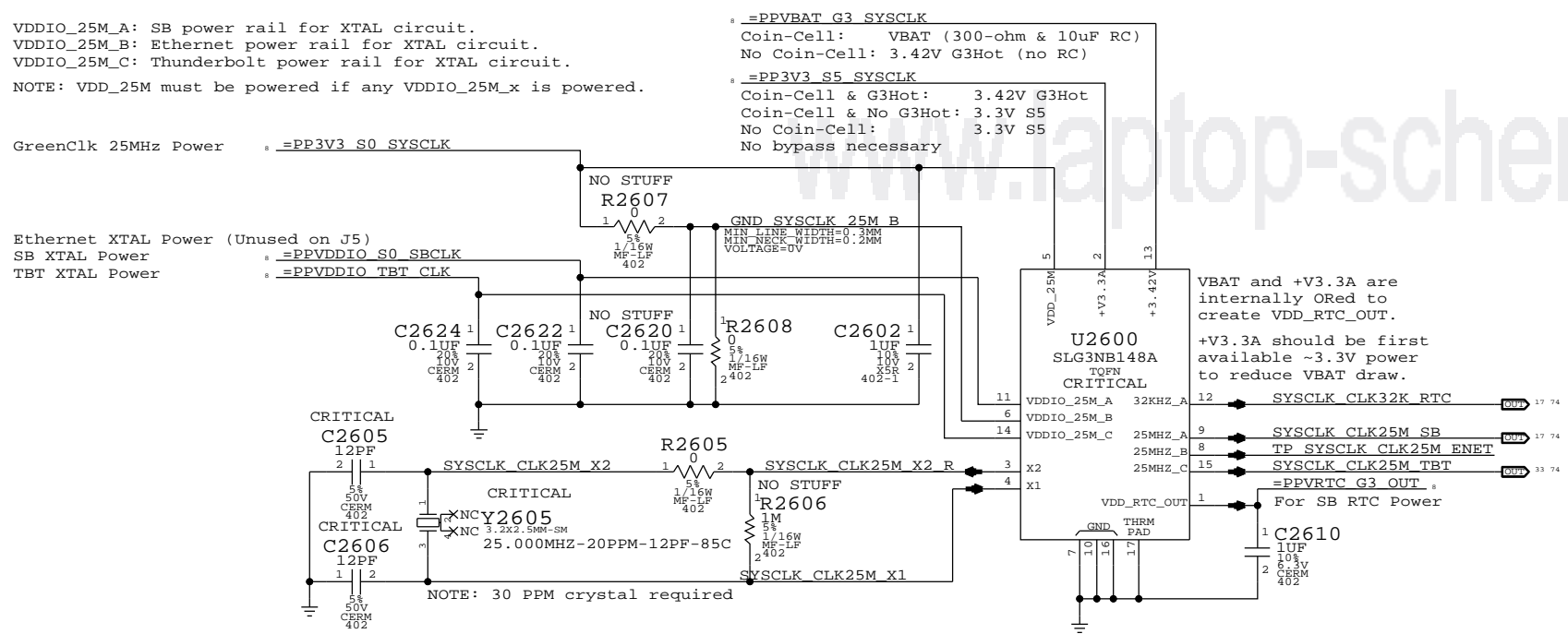
33 MHz Clock Series Termination



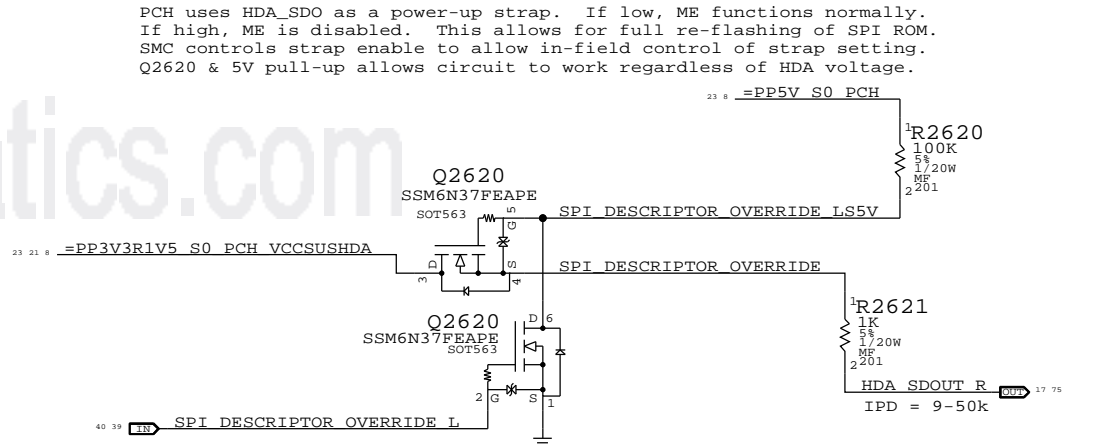
SDCONN_STATE_CHANGE ISOLATION



System RTC Power Source & 32kHz / 25MHz Clock Generator



PCH ME Disable Strap



SYNC MASTER=MASTER		SYNC DATE=MASTER	
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

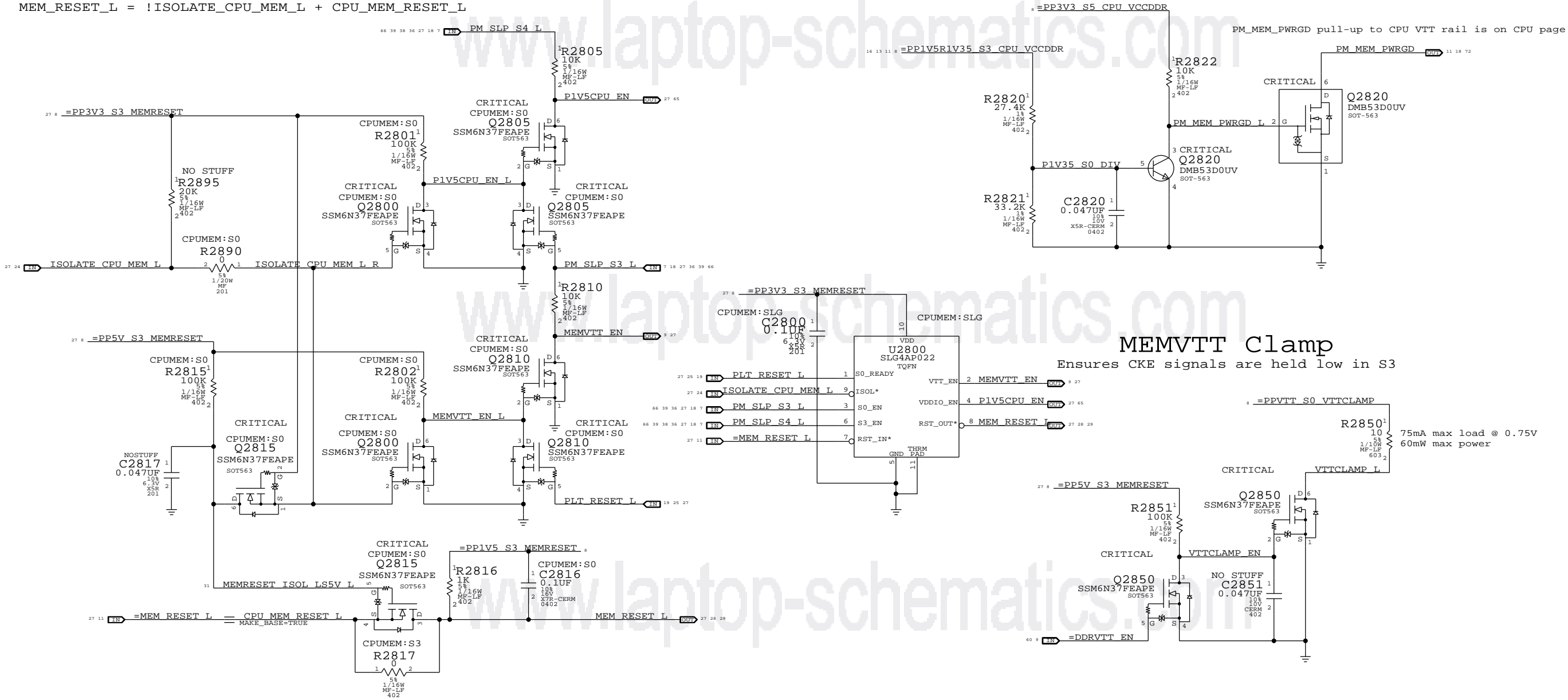
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

1V35 S0 "PGOOD" for CPU



MEMVTT Clamp

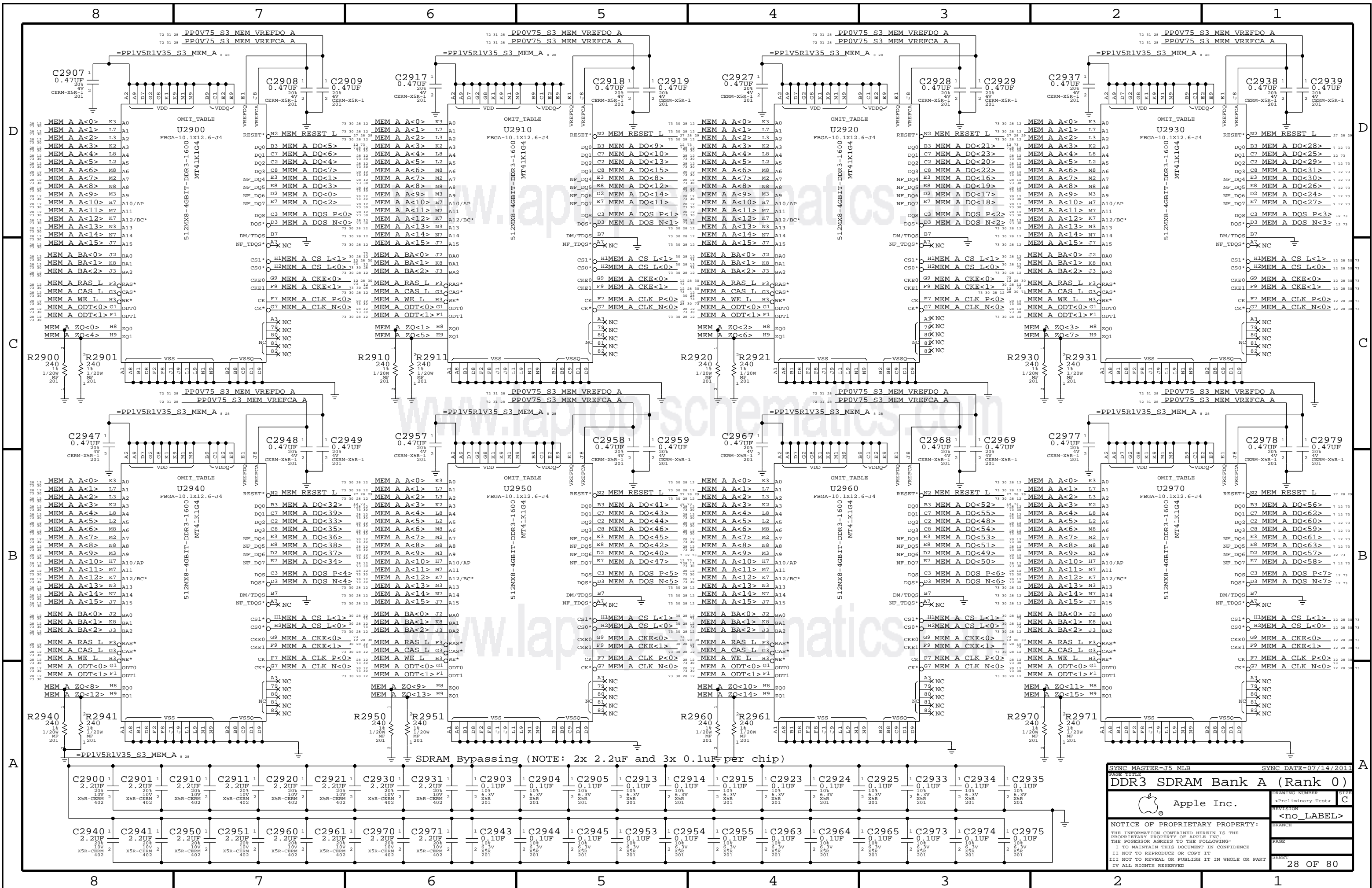
Ensures CKE signals are held low in S3

Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

PAGE TITLE		SYNC DATE=07/29/2011	
CPU Memory S3 Support			
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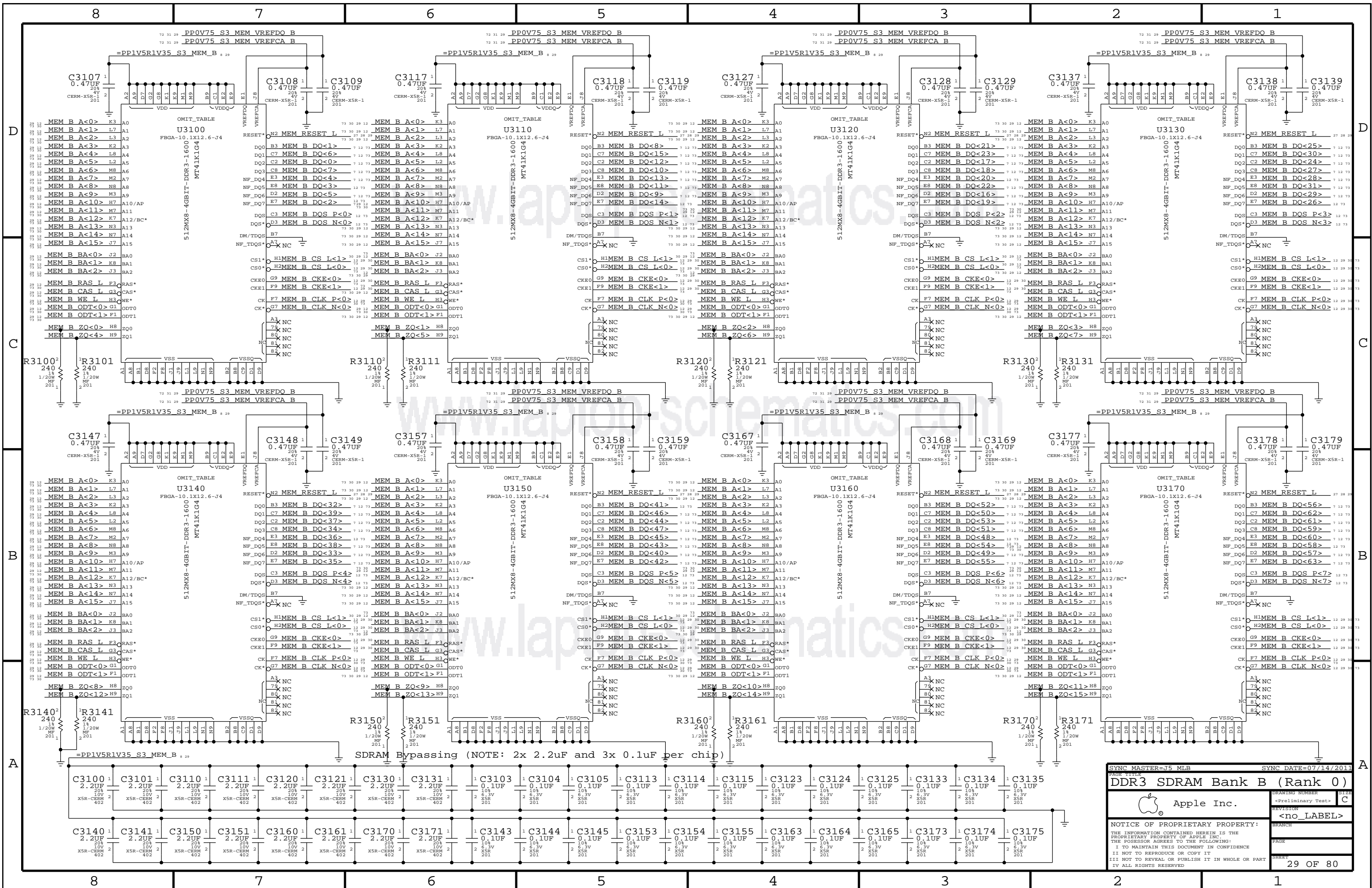


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28 OF 80



SYNC MASTER=J5 MLB

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DDR3 SDRAM Bank B (Rank 0)

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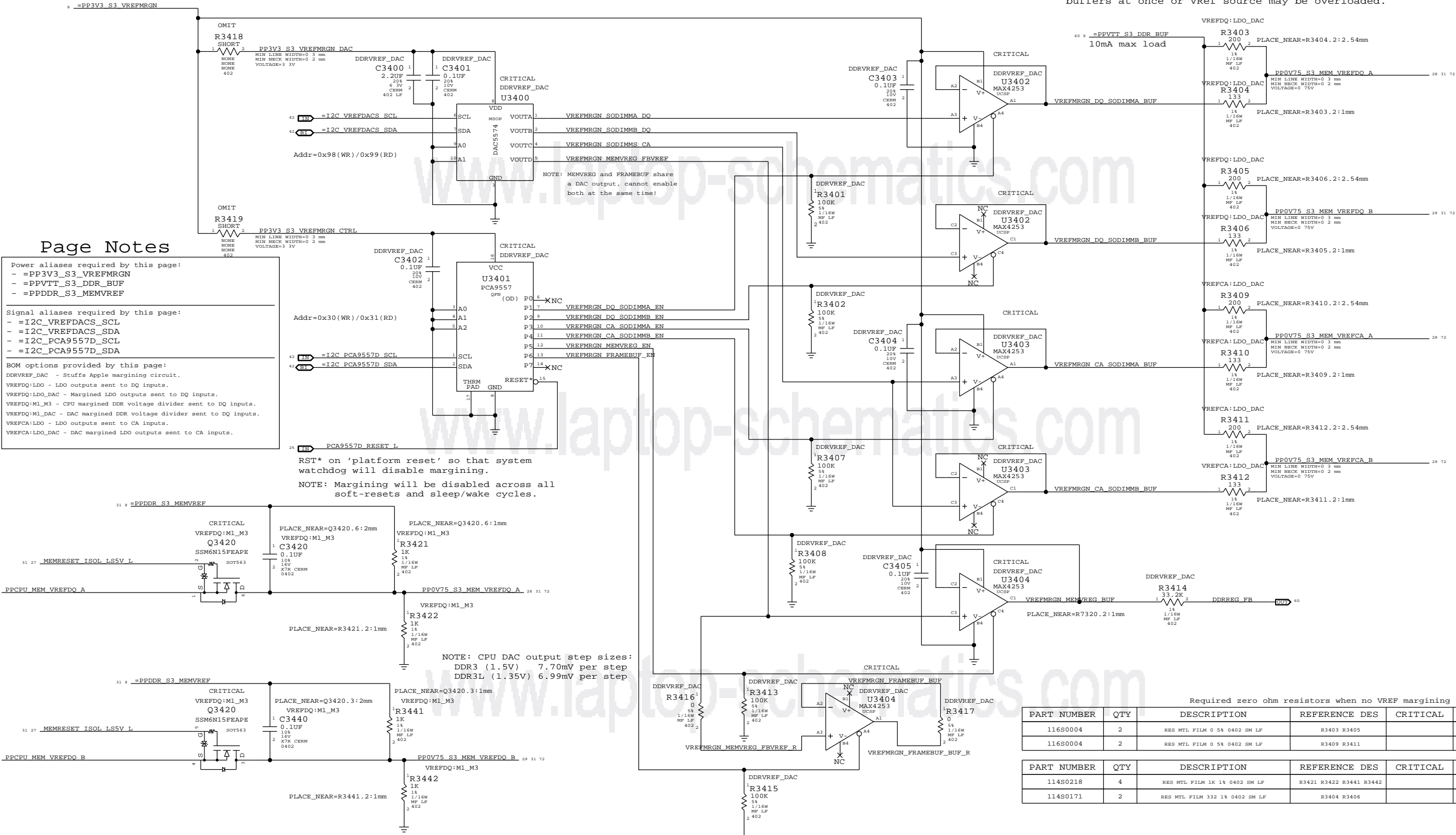
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (= sourced)			+61uA - -61uA (= sourced)	+6.0mA - -5.0mA (= sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J5 MLB

SYNC DATE=07/29/2011

DDR3/FRAMEBUF VREF MARGINING

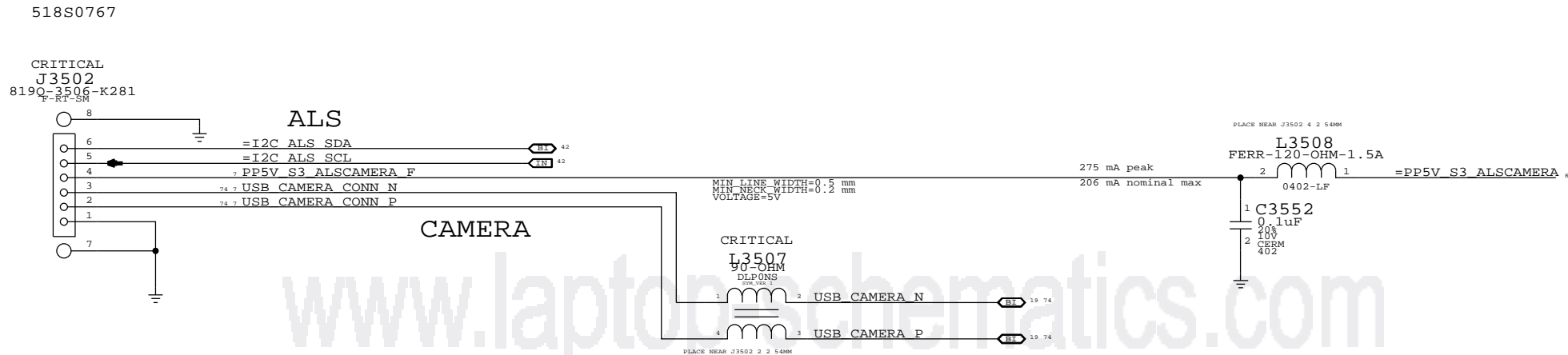
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31 OF 80

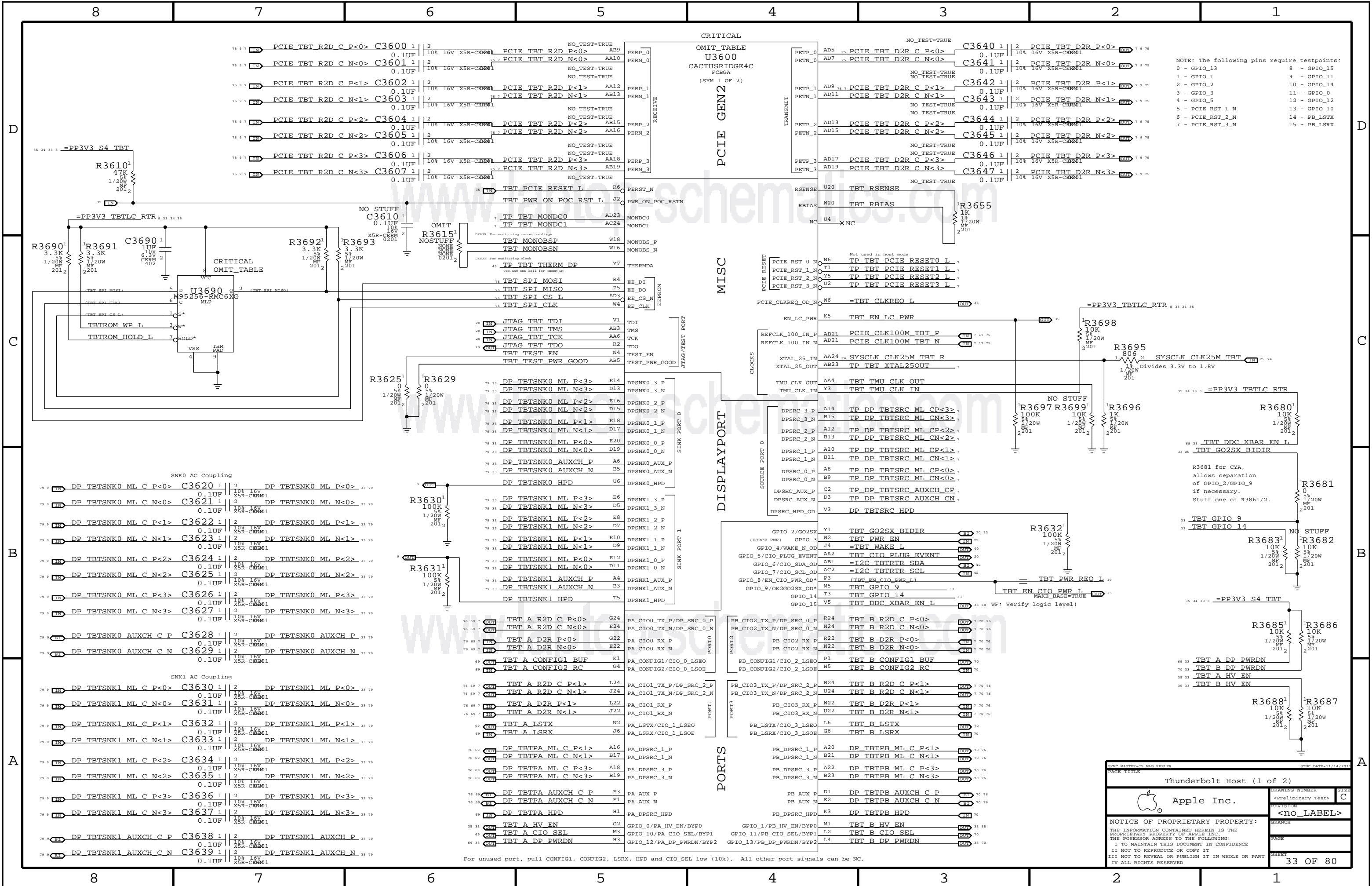
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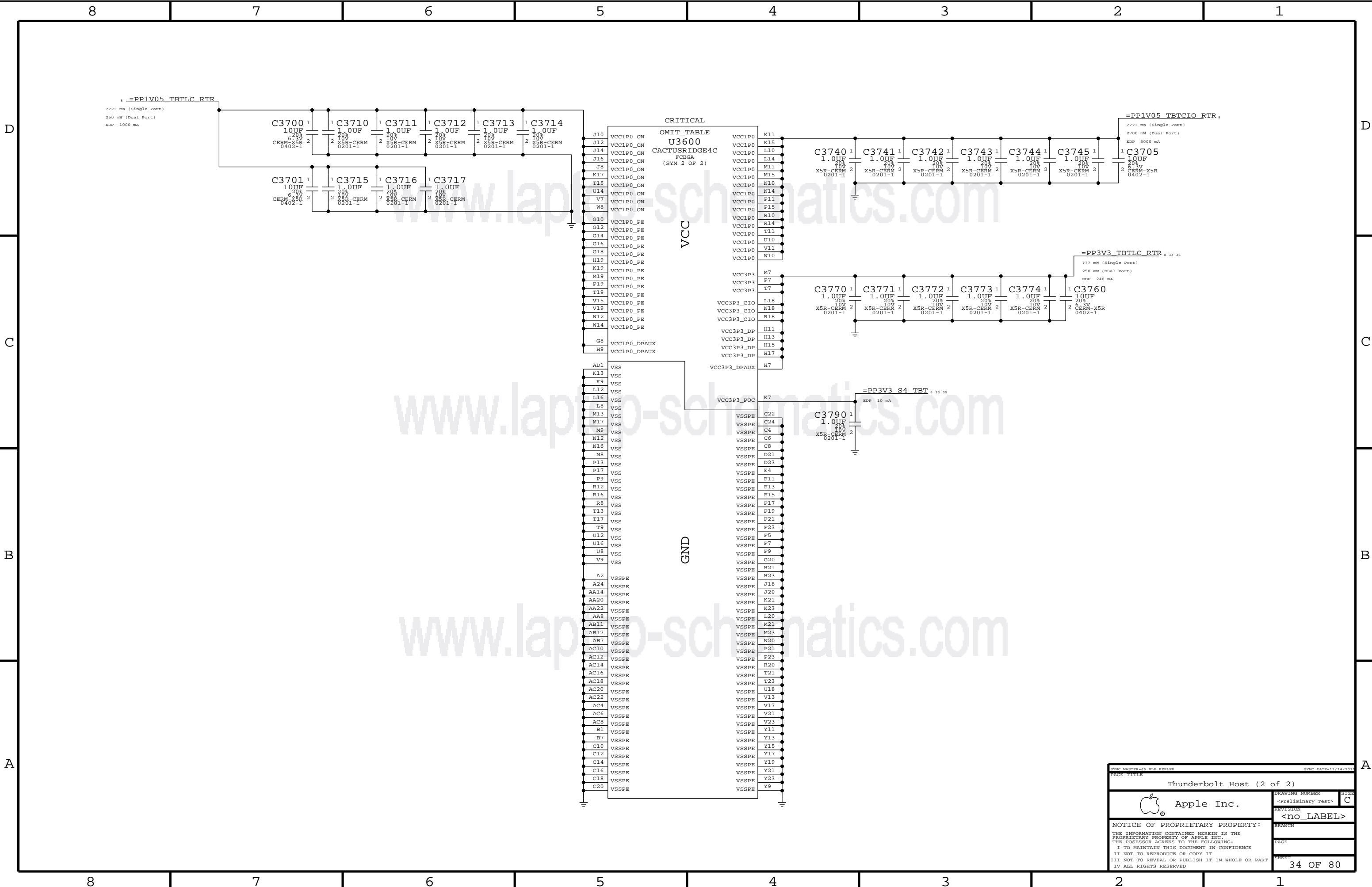


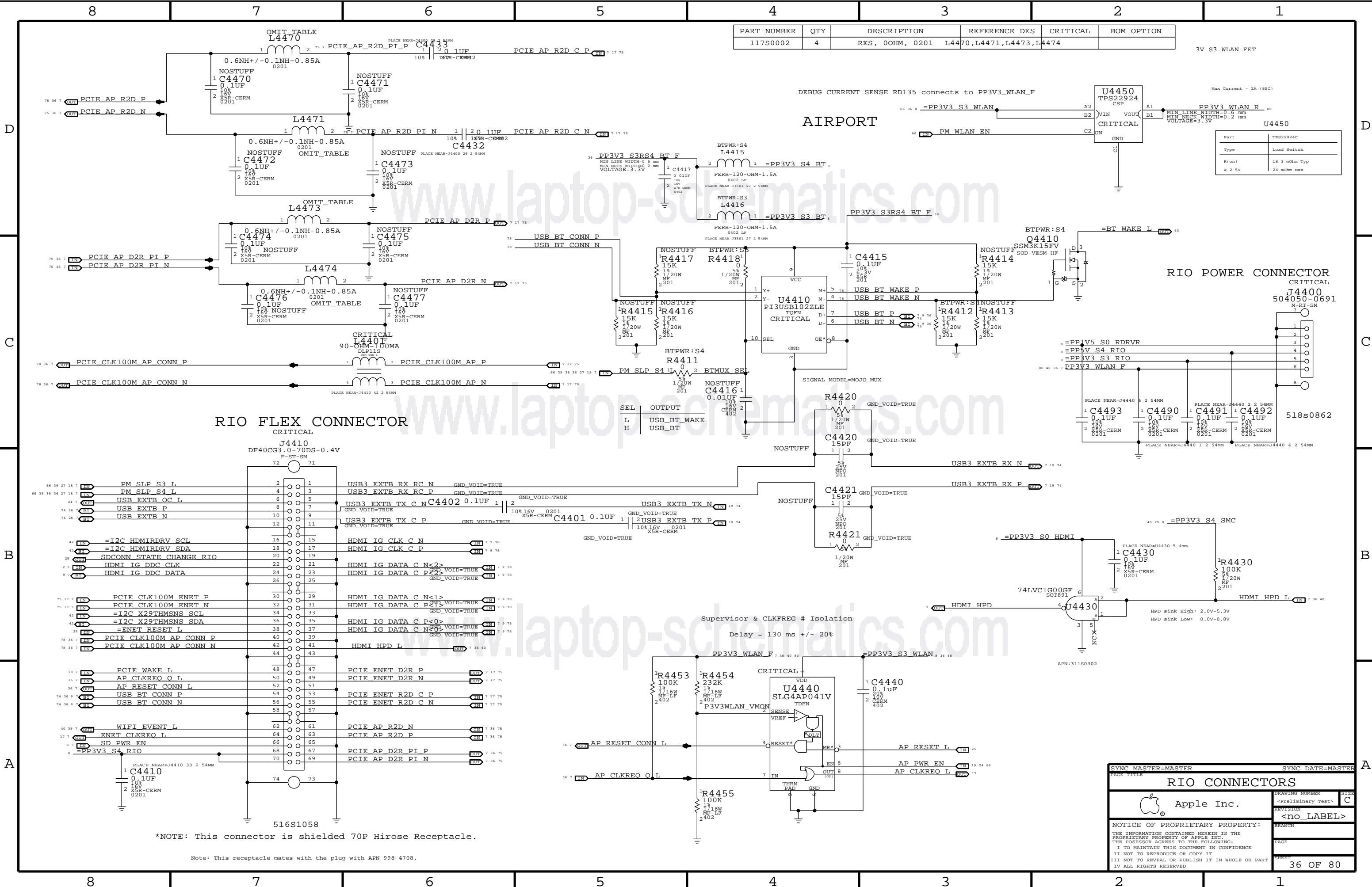
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SYNC MASTER=MASTER		SYNC DATE=MASTER	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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3V S3 WLAN FET

AIRPORT

RIO POWER CONNECTOR

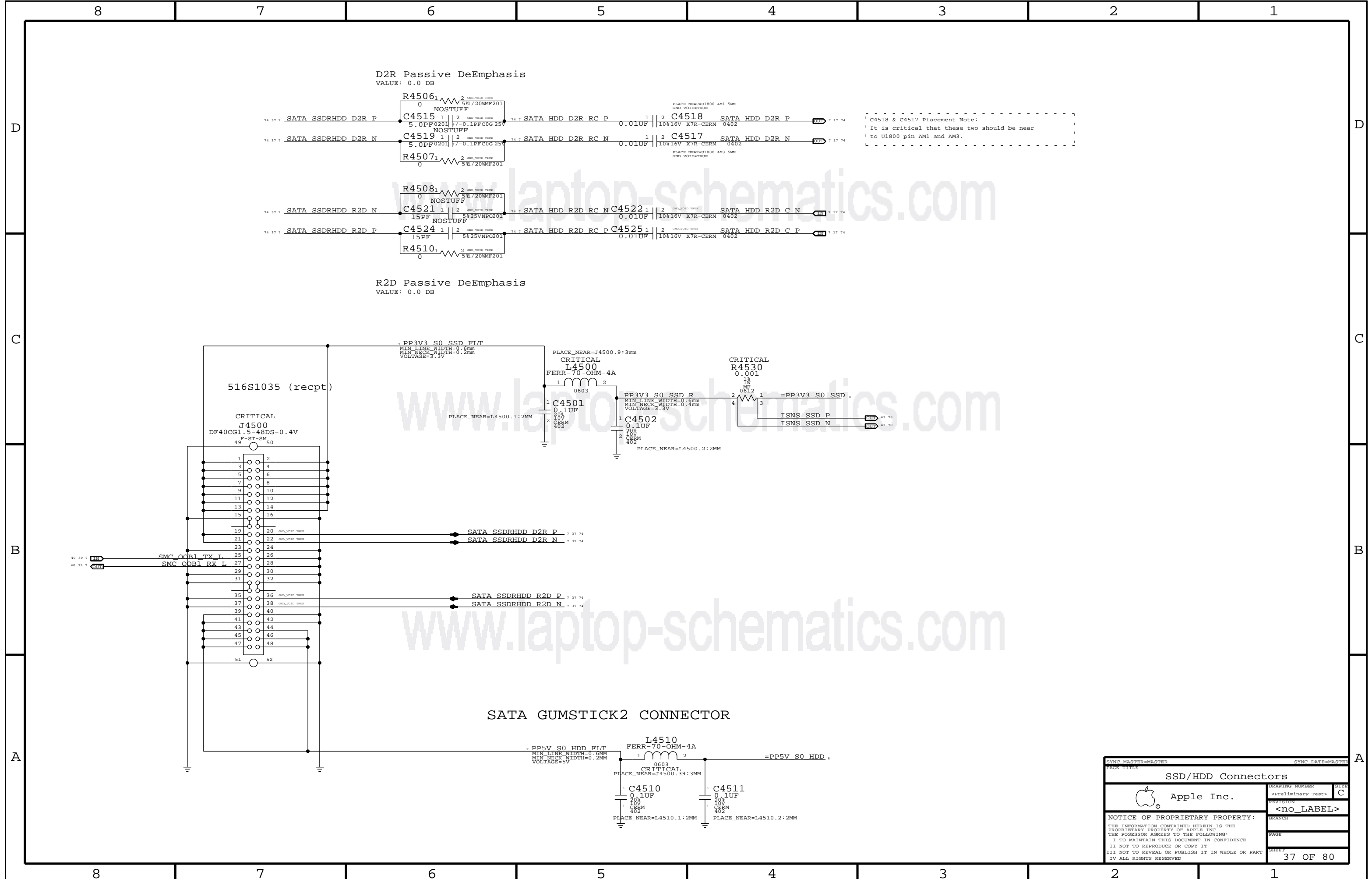
RIO FLEX CONNECTOR

66 39 27 18 1	PM SLP S3 L	2	1	USB3_EXTB_RX_RC_N	GND_VOID=TRUE	19 74
66 39 38 36 27 18 1	PM SLP S4 L	4	3	USB3_EXTB_RX_RC_P	GND_VOID=TRUE	19 74
24	USB_EXTB_OC_L	6	5	USB3_EXTB_TX_C_N	GND_VOID=TRUE	19 74
24	USB_EXTB_P	8	7	USB3_EXTB_TX_C_P	GND_VOID=TRUE	19 74
24	USB_EXTB_N	10	9	USB3_EXTB_TX_P	GND_VOID=TRUE	19 74
42	=I2C_HDMI_RDRV_SCL	16	15	HDMI_IG_CLK_C_N	GND_VOID=TRUE	7 9 78
42	=I2C_HDMI_RDRV_SDA	18	17	HDMI_IG_CLK_C_P	GND_VOID=TRUE	7 9 78
25	SDCONN_STATE_CHANGE_RIO	20	19	HDMI_IG_DATA_C_N<2>	GND_VOID=TRUE	7 9 78
9 7	HDMI_IG_DDC_CLK	22	21	HDMI_IG_DATA_C_P<2>	GND_VOID=TRUE	7 9 78
9 7	HDMI_IG_DDC_DATA	24	23	HDMI_IG_DATA_C_N<1>	GND_VOID=TRUE	7 9 78
75 17 7	PCIE_CLK100M_ENET_P	30	29	HDMI_IG_DATA_C_P<1>	GND_VOID=TRUE	7 9 78
75 17 7	PCIE_CLK100M_ENET_N	32	31	HDMI_IG_DATA_C_P<0>	GND_VOID=TRUE	7 9 78
42	=I2C_X29THMSNS_SCL	34	33	HDMI_HPDL		36 40
42	=I2C_X29THMSNS_SDA	36	35	PCIE_ENET_D2R_P		7 17 75
25	=ENET_RESET_L	38	37	PCIE_ENET_D2R_N		7 17 75
78 36 7	PCIE_CLK100M_AP_CONN_P	40	39	PCIE_AP_R2D_P		7 36 75
78 36 7	PCIE_CLK100M_AP_CONN_N	42	41	PCIE_AP_R2D_N		7 36 75
18 7	PCIE_WAKE_L	48	47	PCIE_AP_D2R_PI_P		7 36 75
36 7	AP_CLKREQ_O_L	50	49	PCIE_AP_D2R_PI_N		7 36 75
36 7	AP_RESET_CONN_L	52	51			
74 36 9	USB_BT_CONN_P	54	53			
74 36 9	USB_BT_CONN_N	56	55			
40 39 7	WIFI_EVENT_L	62	61			
17 7	ENET_CLKREQ_L	64	63			
9 7	SD_PWR_EN	66	65			
8	=PP3V3_S4_RIO	68	67			
		70	69			

*NOTE: This connector is shielded 70P Hirose Receptacle.

Note: This receptacle mates with the plug with APN 998-4708.


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RIO CONNECTORS		<Preliminary Test>	
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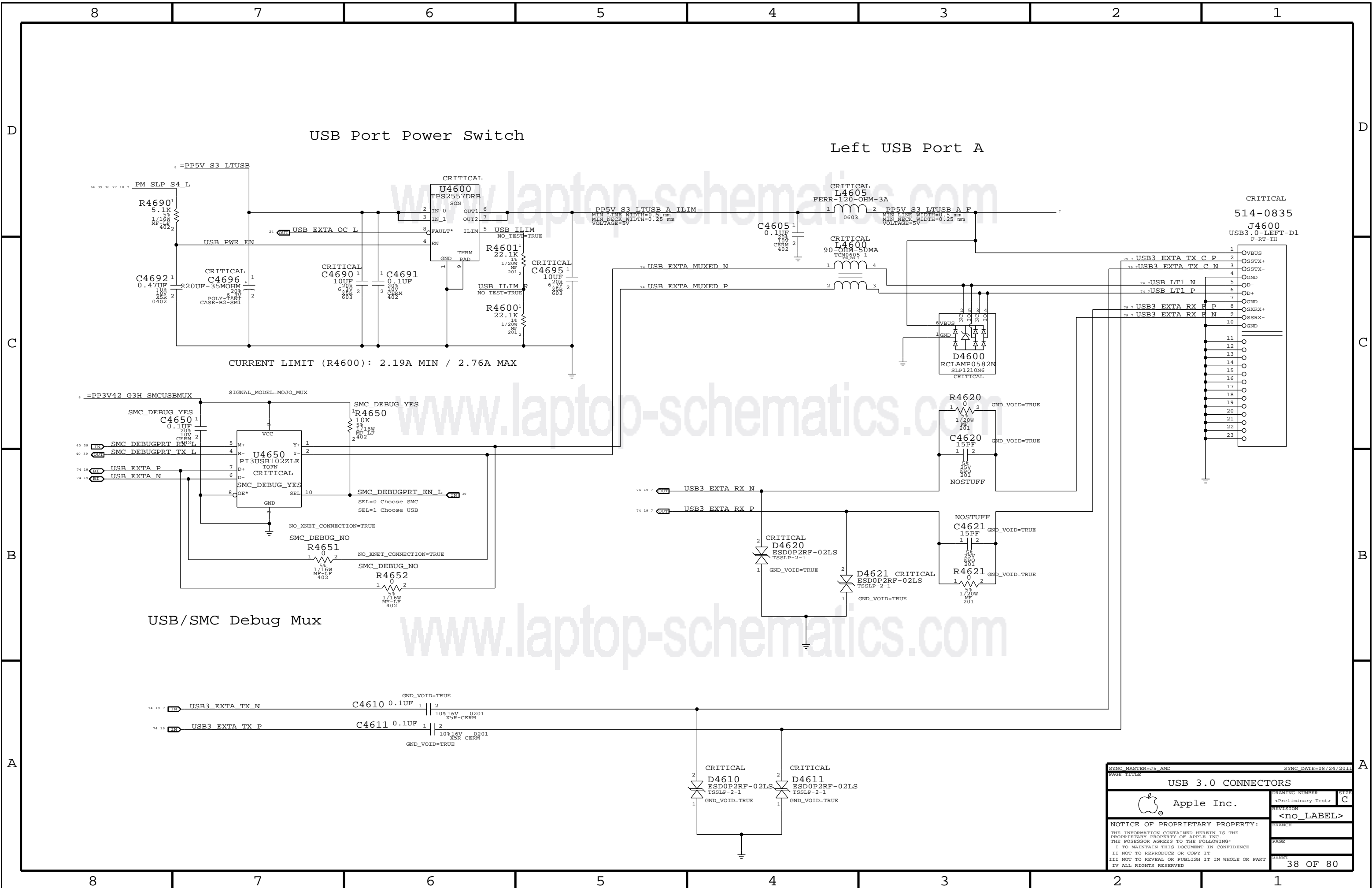


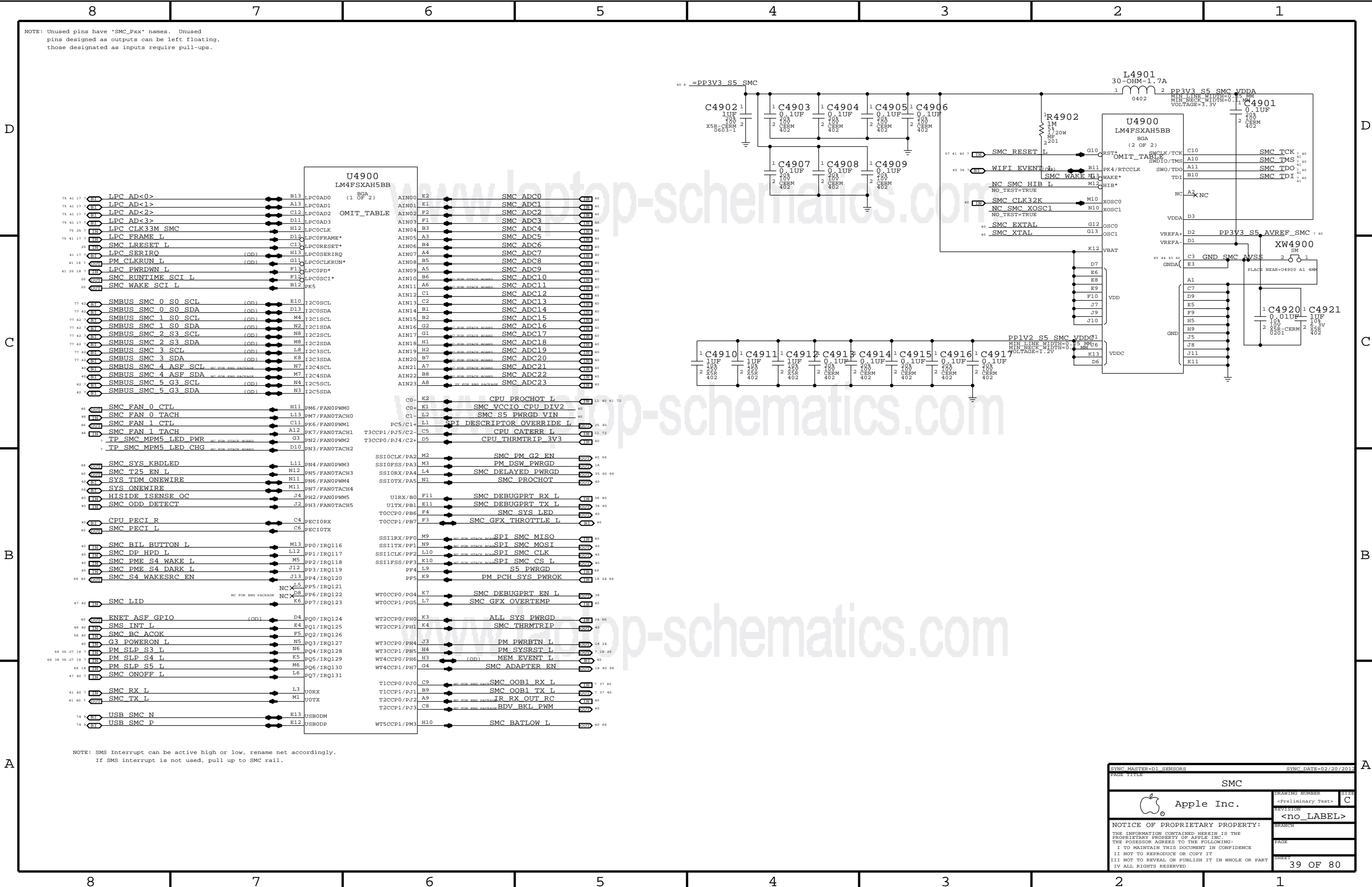
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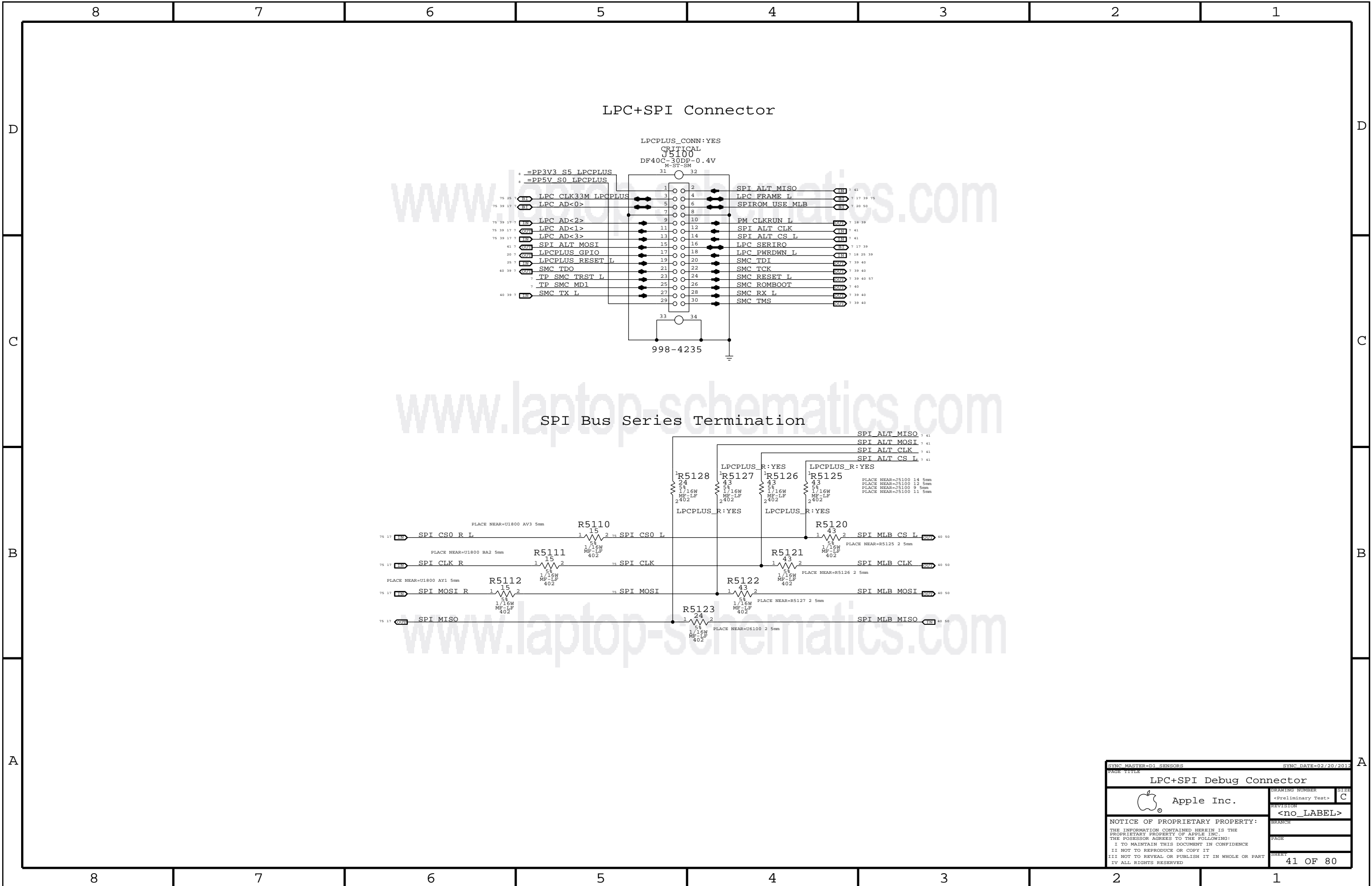
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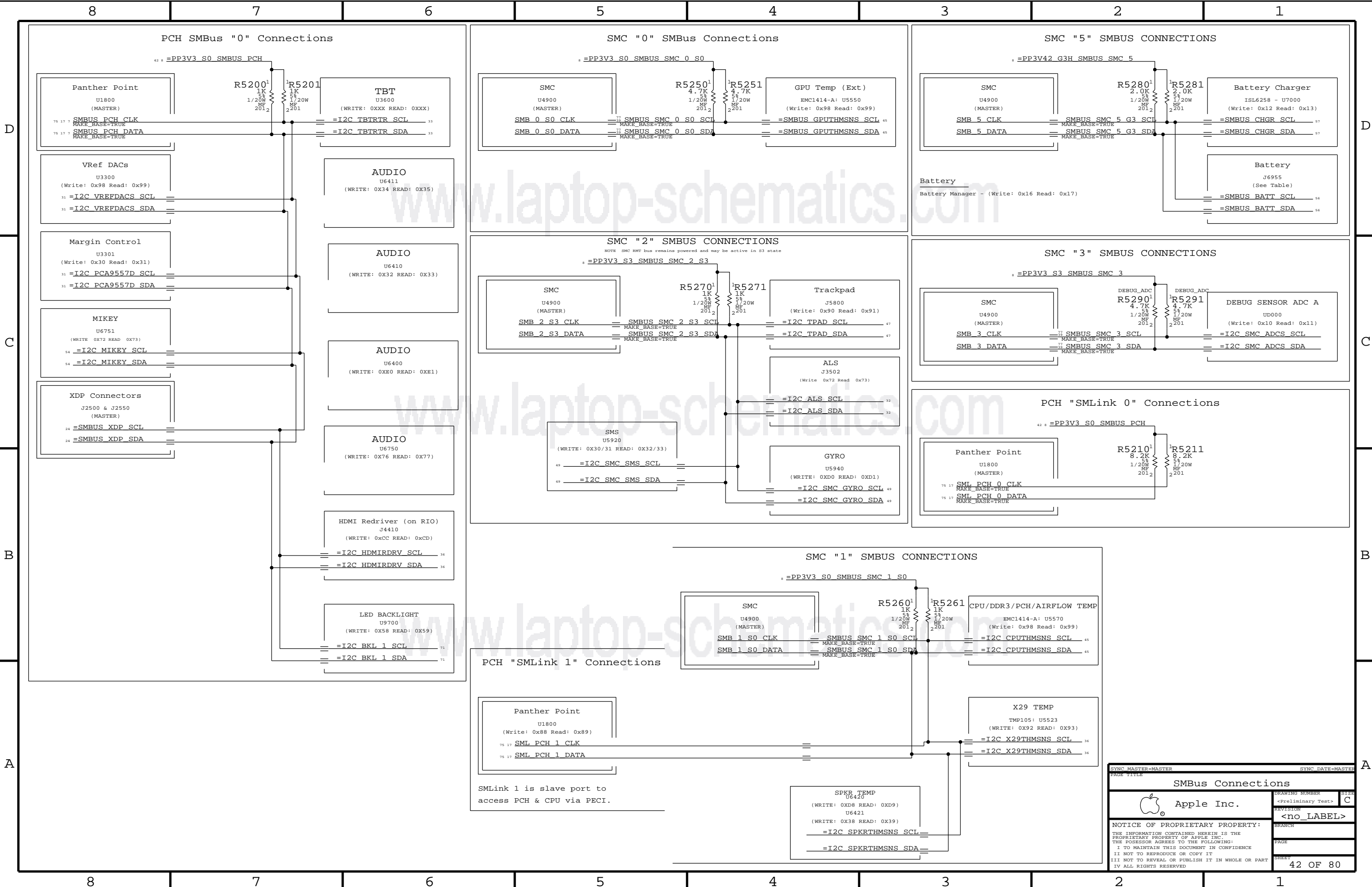
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SSD/HDD Connectors			
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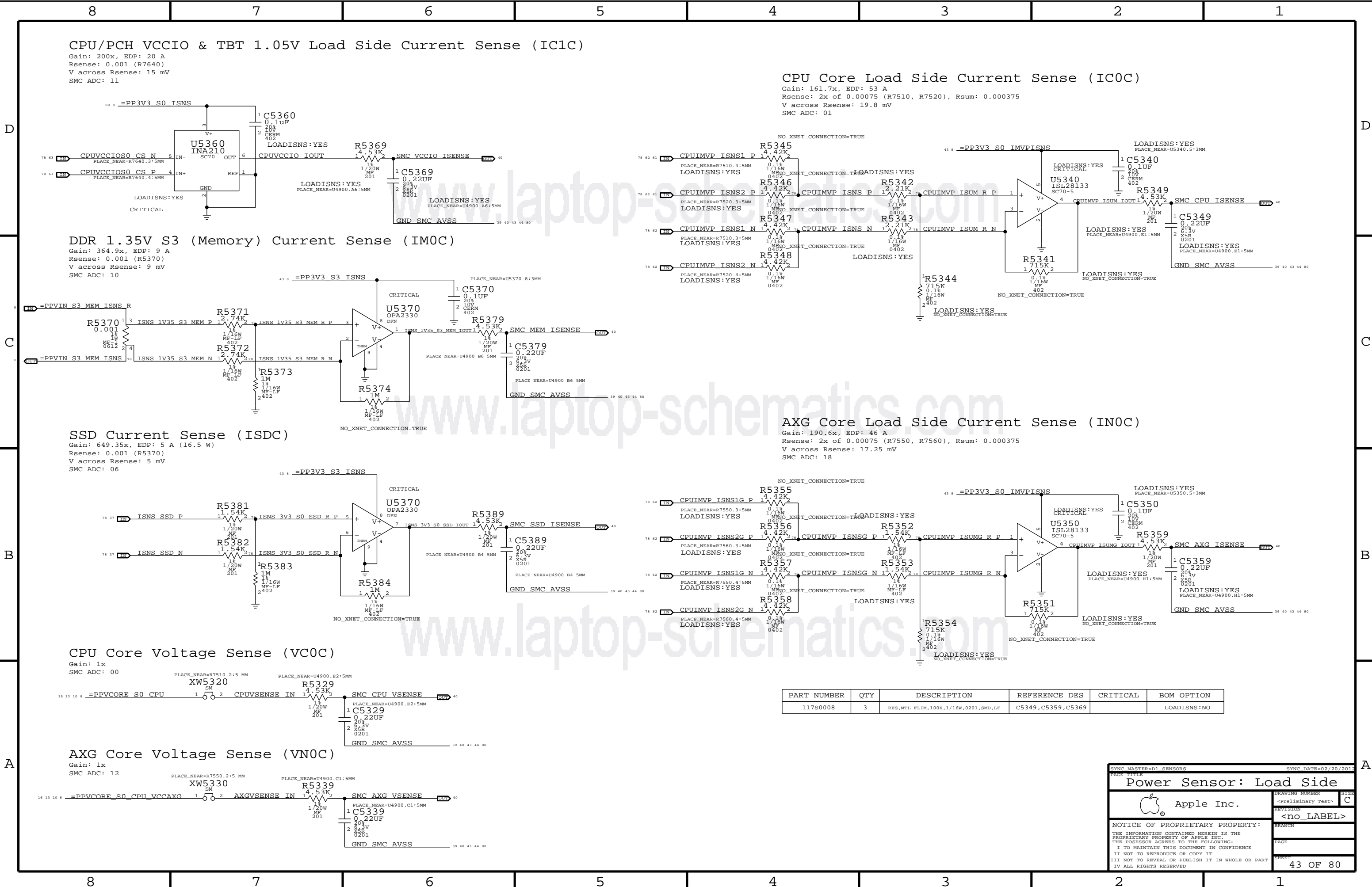




SYNC MASTER=D1 SENSORS		SYNC DATE=02/20/2012	
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SMC			
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	BRANCH		
	PAGE		
	SHEET		
39			OF 80







PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC MASTER=D1 SENSORS

SYNC DATE=03/20/2012

Power Sensor: Load Side

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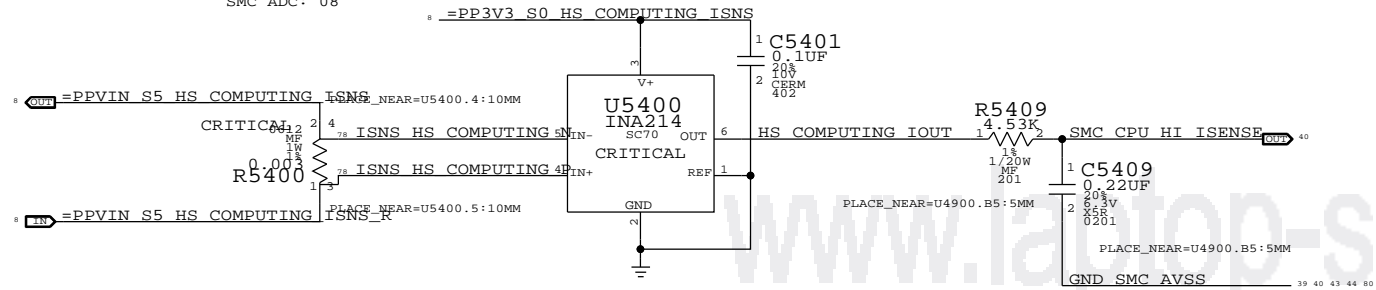
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43 OF 80

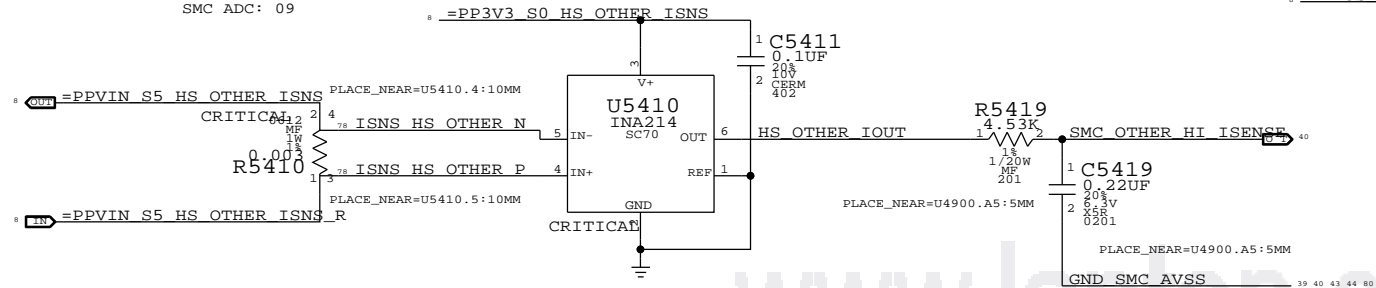
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
SMC ADC: 08



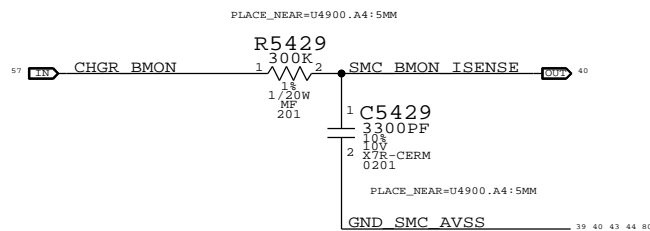
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
SMC ADC: 09



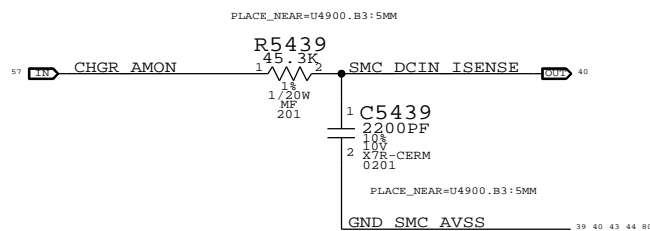
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
Rsense: 0.010 (R7050)
SMC ADC: 07



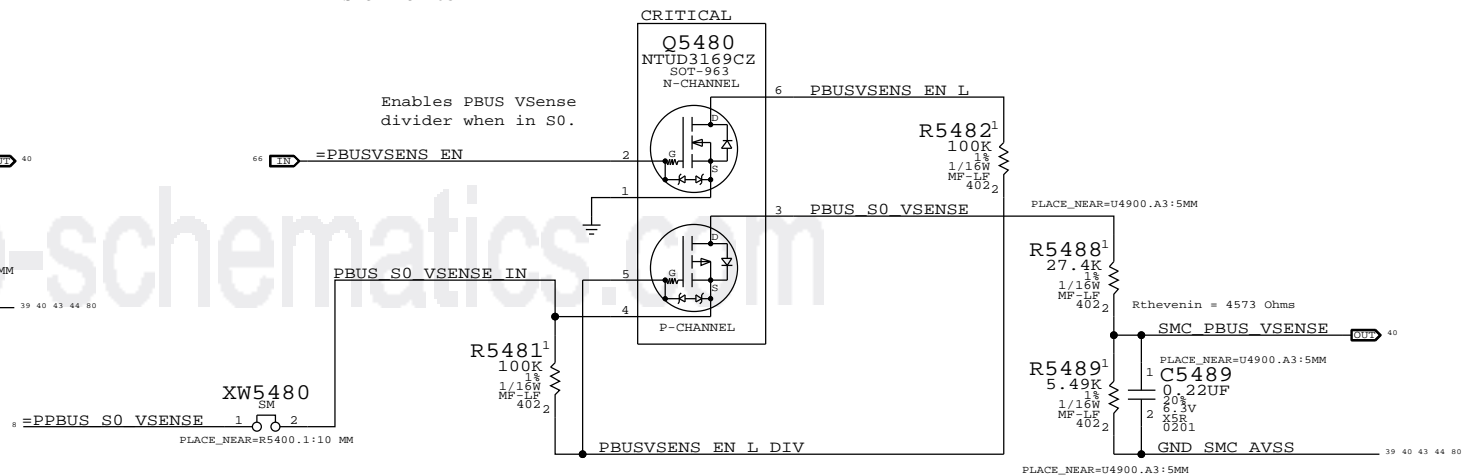
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 04



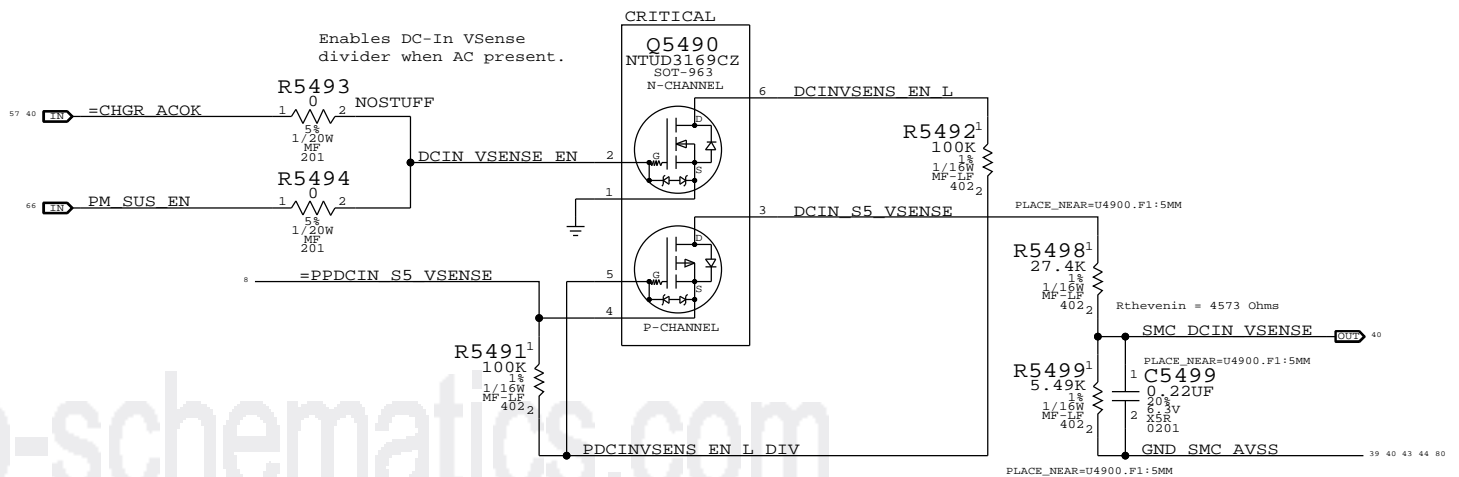
PBUS Voltage Sense & Enable (VP0R)


Gain: 0.167x
SMC ADC: 05

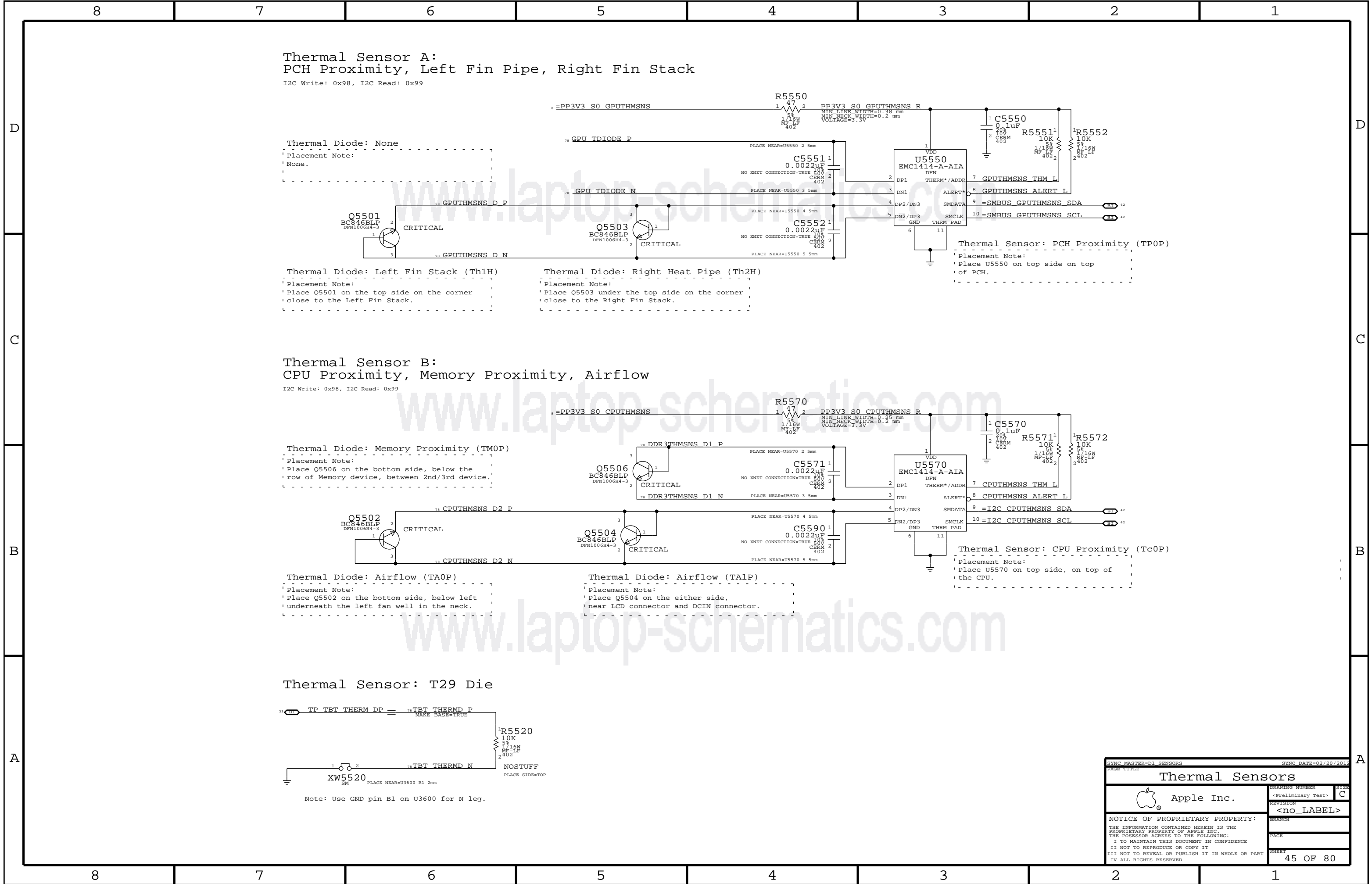



DC In Voltage Sense & Enable (VD0R)

Gain: 0.167x
SMC ADC: 03

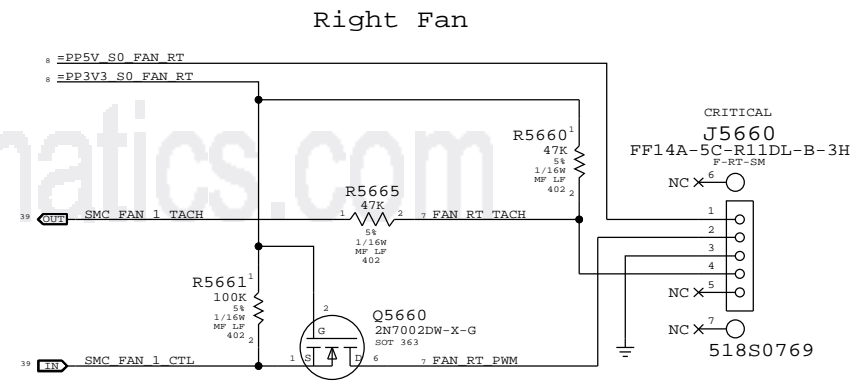
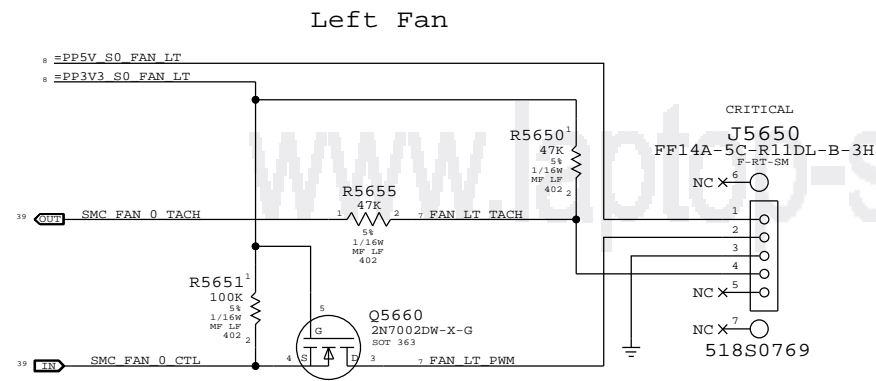


SYNC MASTER=D1 SENSORS		SYNC DATE=02/20/2012	
PAGE TITLE			
Power Sensor: High Side			
 Apple Inc.		DRAWING NUMBER <Preliminary Test>	SIZE C
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Thermal Sensors			
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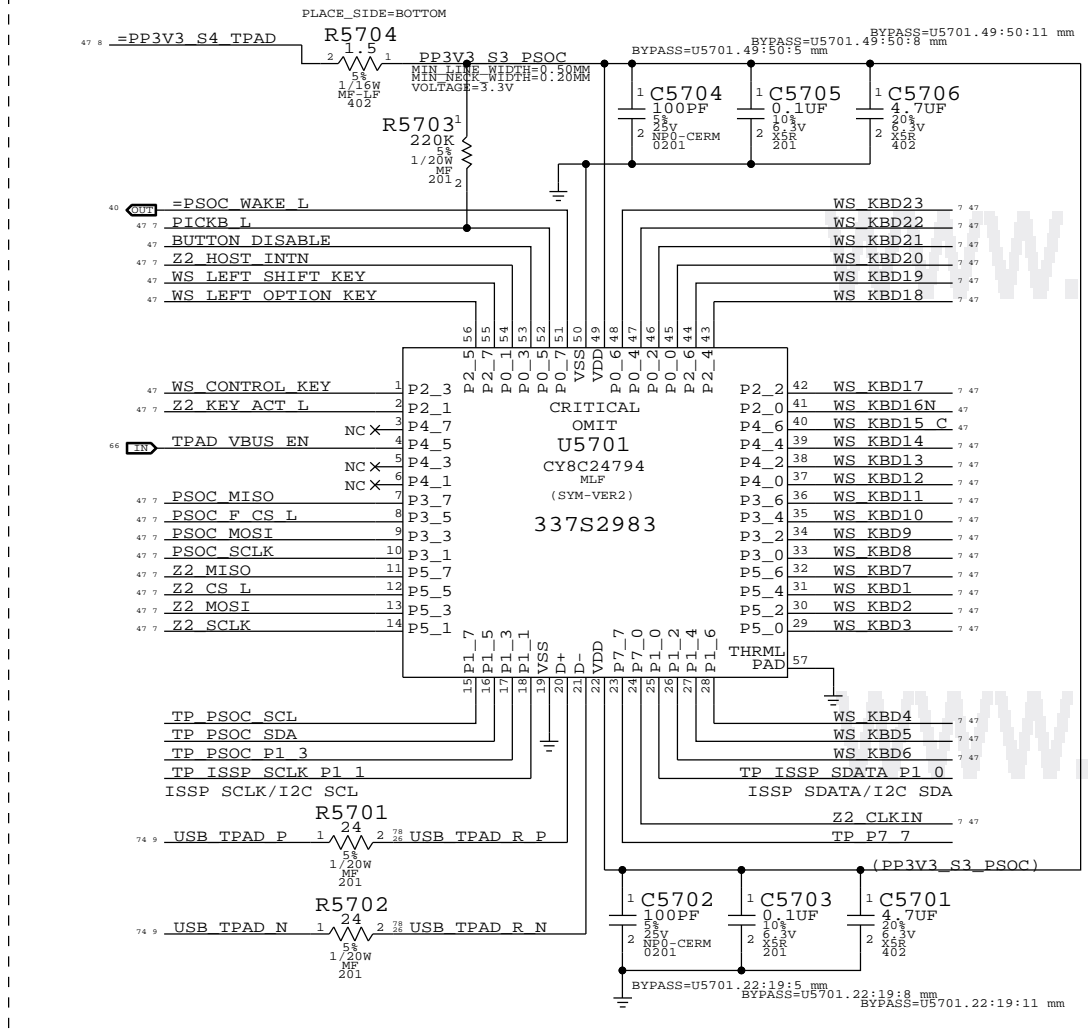
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SYNC MASTER=J5 MLB		SYNC DATE=07/29/2011	
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		PAGE	
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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

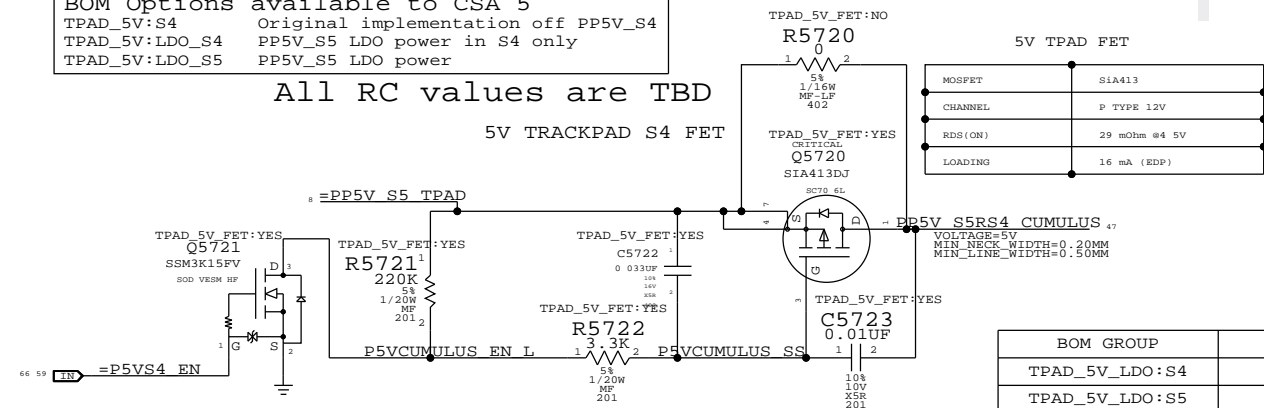


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	VOUT	80UA	0.204 V	16.32E-6 W	
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.72E-3 W	
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	VDD	14MA (MAX)	0.021 V	294E-6 W	
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

BOM Options available to CSA 5
TPAD_5V:S4 Original implementation off PP5V_S4
TPAD_5V:LDO_S4 PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5 PP5V_S5 LDO power

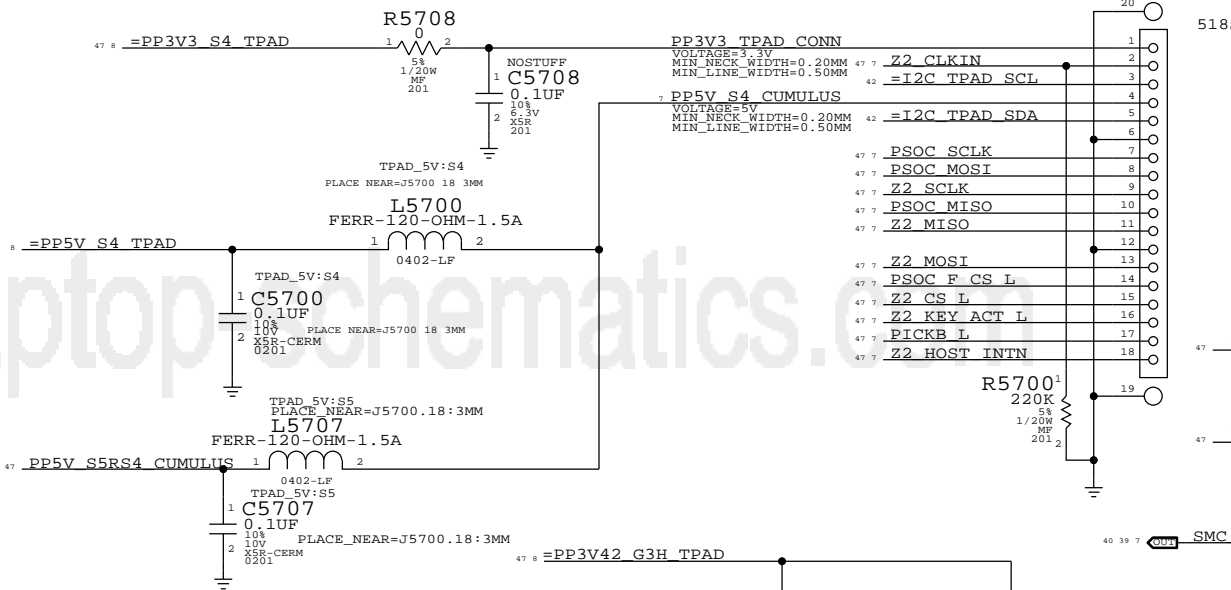
All RC values are TBD

5V TRACKPAD S4 FET

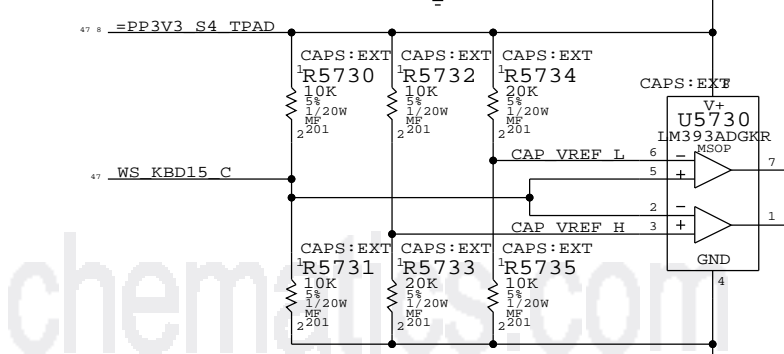
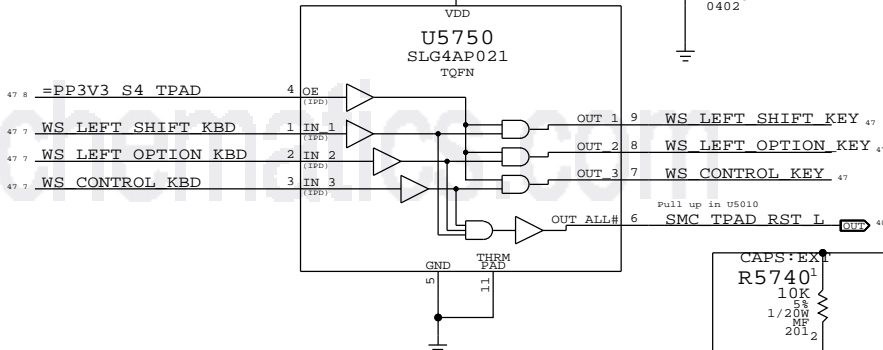


BOM GROUP	BOM OPTIONS
TPAD_5V_LDO:S4	TPAD_5V_FET:YES, TPAD_5V:S5
TPAD_5V_LDO:S5	TPAD_5V_FET:NO, TPAD_5V:S5

IPD Flex Connector



www.qdzbwx.com



WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

CRITICAL J5700

FF14-18C-R11DL

F-RT-SM

518S0848

CRITICAL

J5700

FF14-18C-R11DL

F-RT-SM

518S0848

CRITICAL

J5700

FF14-18C-R11DL

F-RT-SM

518S0848

CRITICAL

J5700

FF14-18C-R11DL

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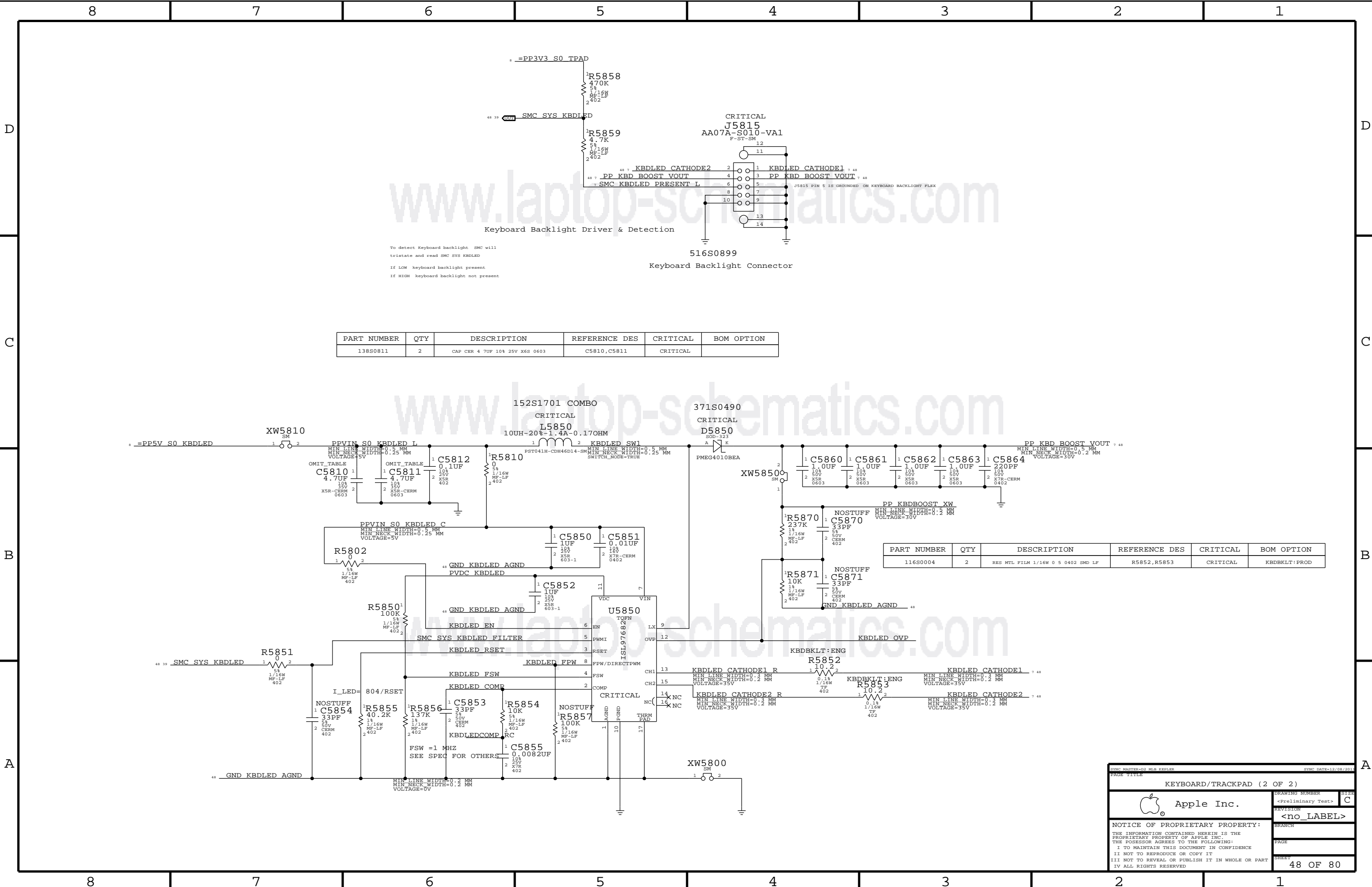
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FF14-18C-R11DL

F-RT-SM

518S0848

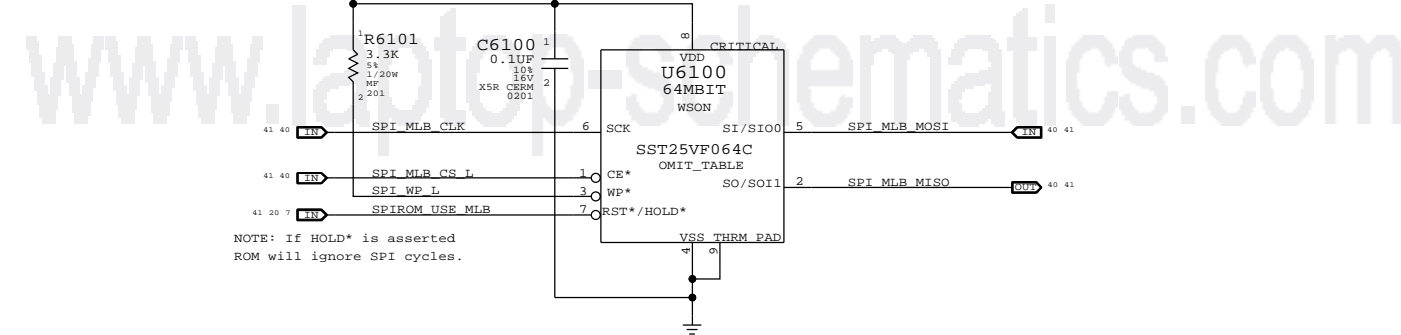


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP CER 4 7UF 10% 25V X6S 0603	C5810,C5811	CRITICAL	


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES MTL FILM 1/16W 0 5 0402 SMD LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

KEYBOARD/TRACKPAD (2 OF 2)	
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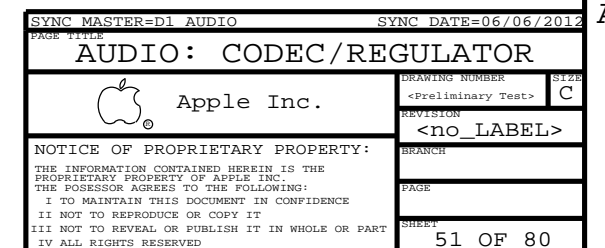


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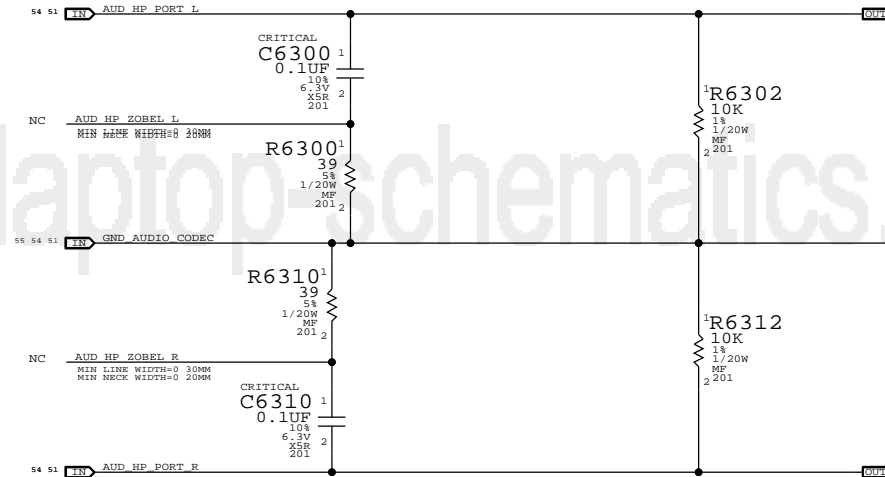


```
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS
```




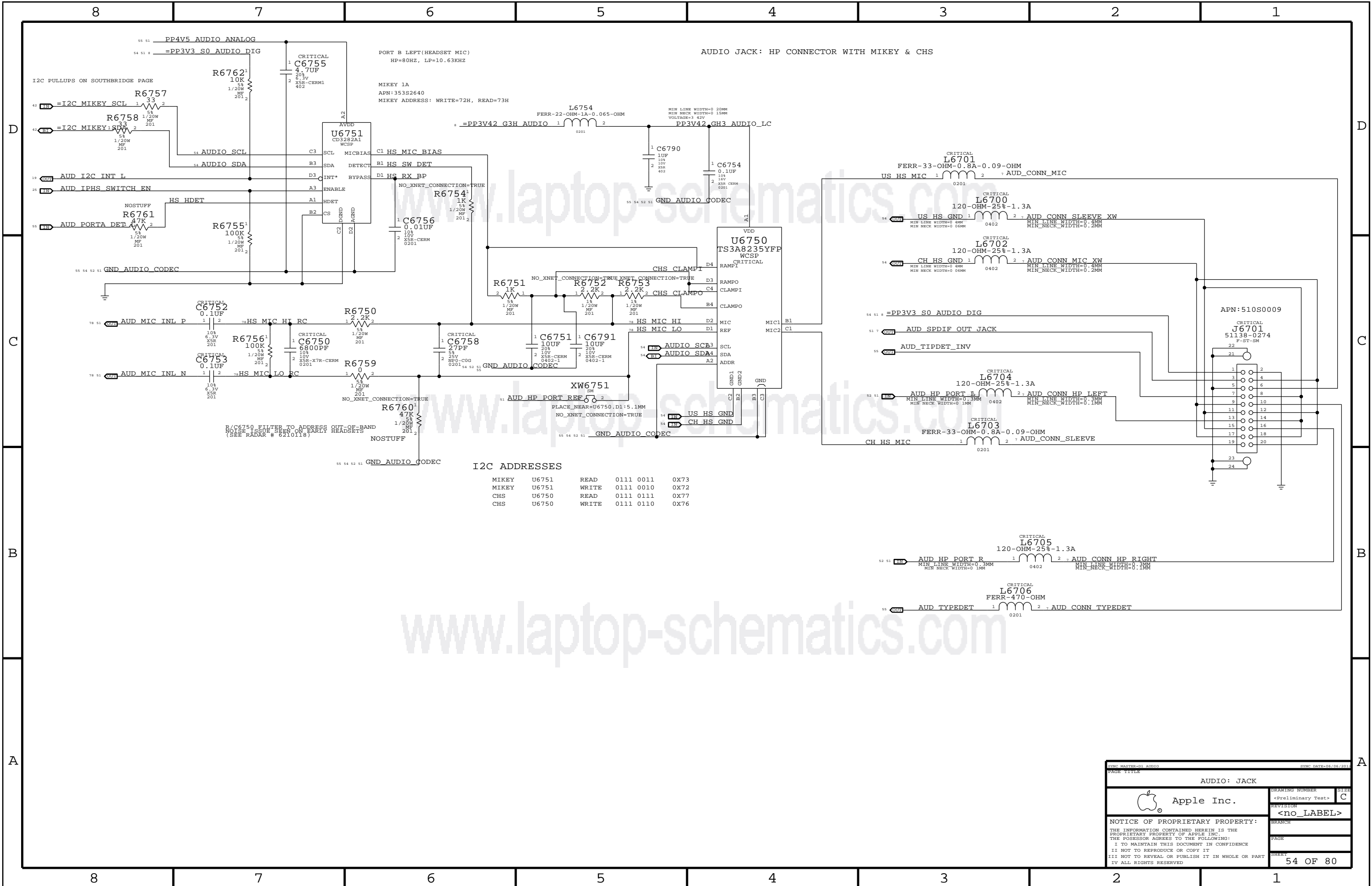
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ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



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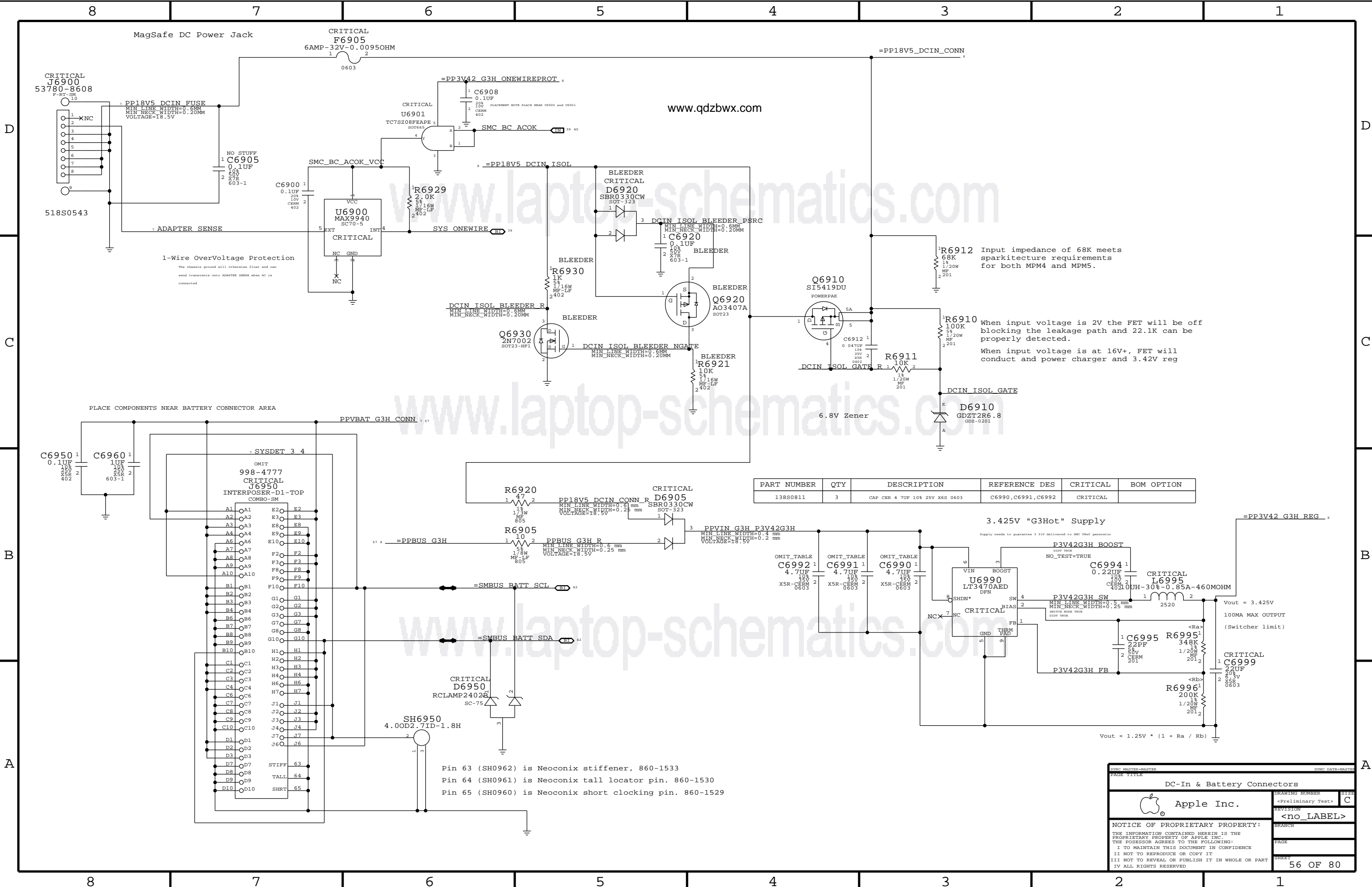
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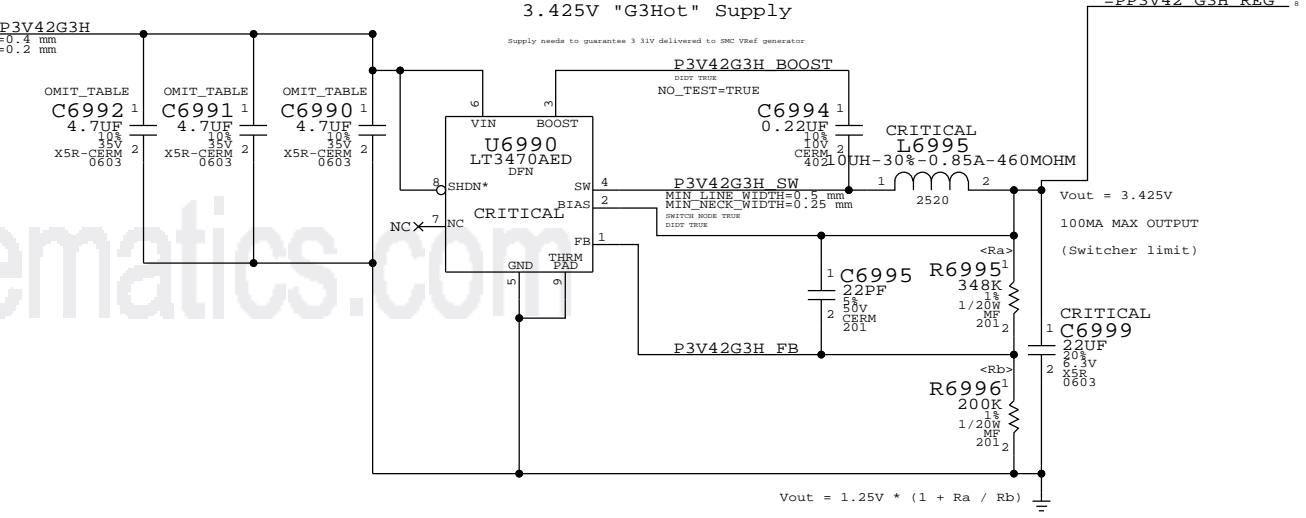
I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

AUDIO: JACK		DRAWING NUMBER	SIZE
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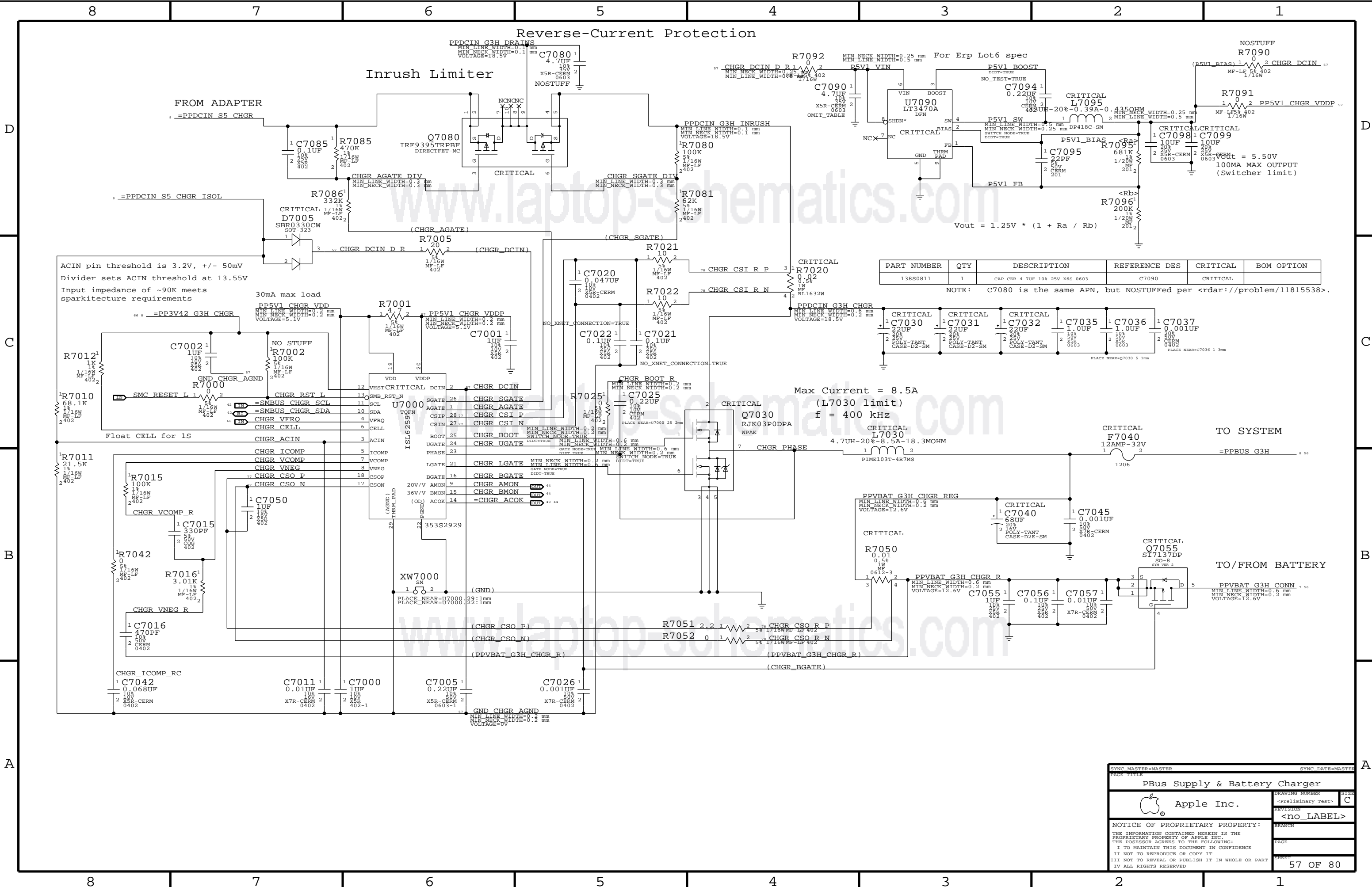


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP CER 4 7UF 10% 25V X6S 0603	C6990,C6991,C6992	CRITICAL	




Pin 63 (SH0962) is Neoconix stiffener, 860-1533
Pin 64 (SH0961) is Neoconix tall locator pin. 860-1530
Pin 65 (SH0960) is Neoconix short clocking pin. 860-1529

PAGE TITLE		PAGE TITLE	
DC-In & Battery Connectors		DC-In & Battery Connectors	
Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	C
		BRANCH	
		PAGE	
		SHEET	
		56 OF 80	



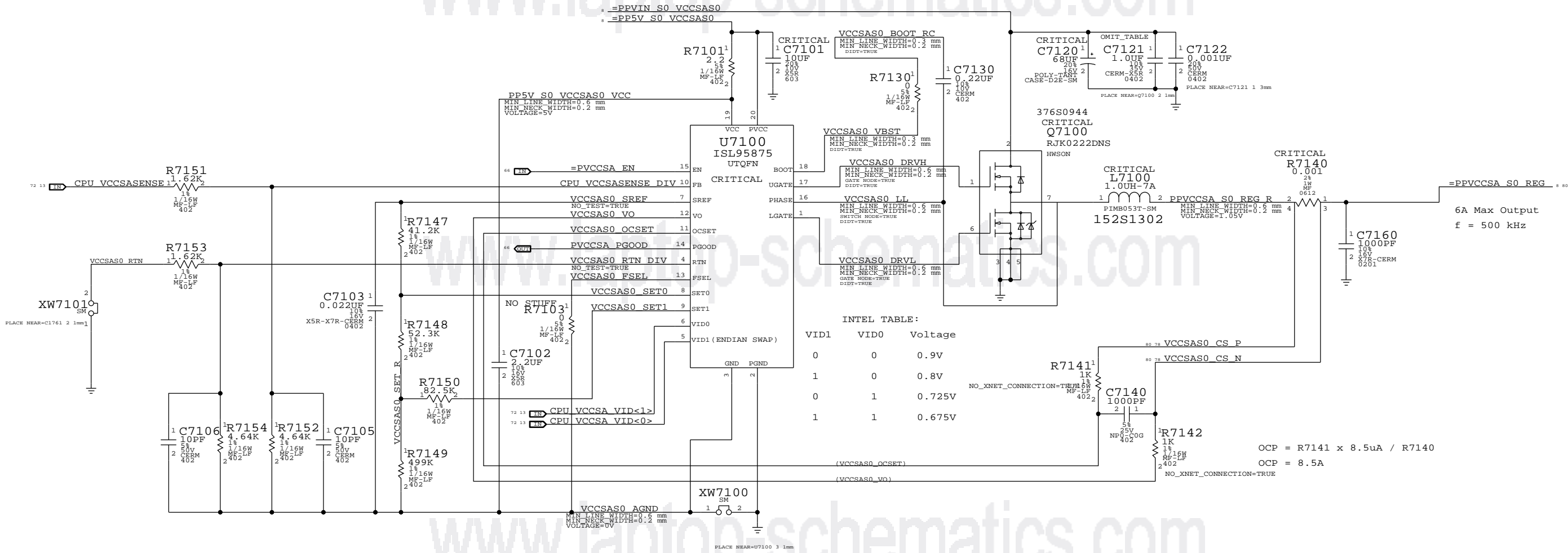
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138S0811	1	CAP CER 4 7UF 10% 25V X6S 0603	C7090	CRITICAL	


NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

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PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	SIZE
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		SHEET	
		57 OF 80	

System Agent Power Supply

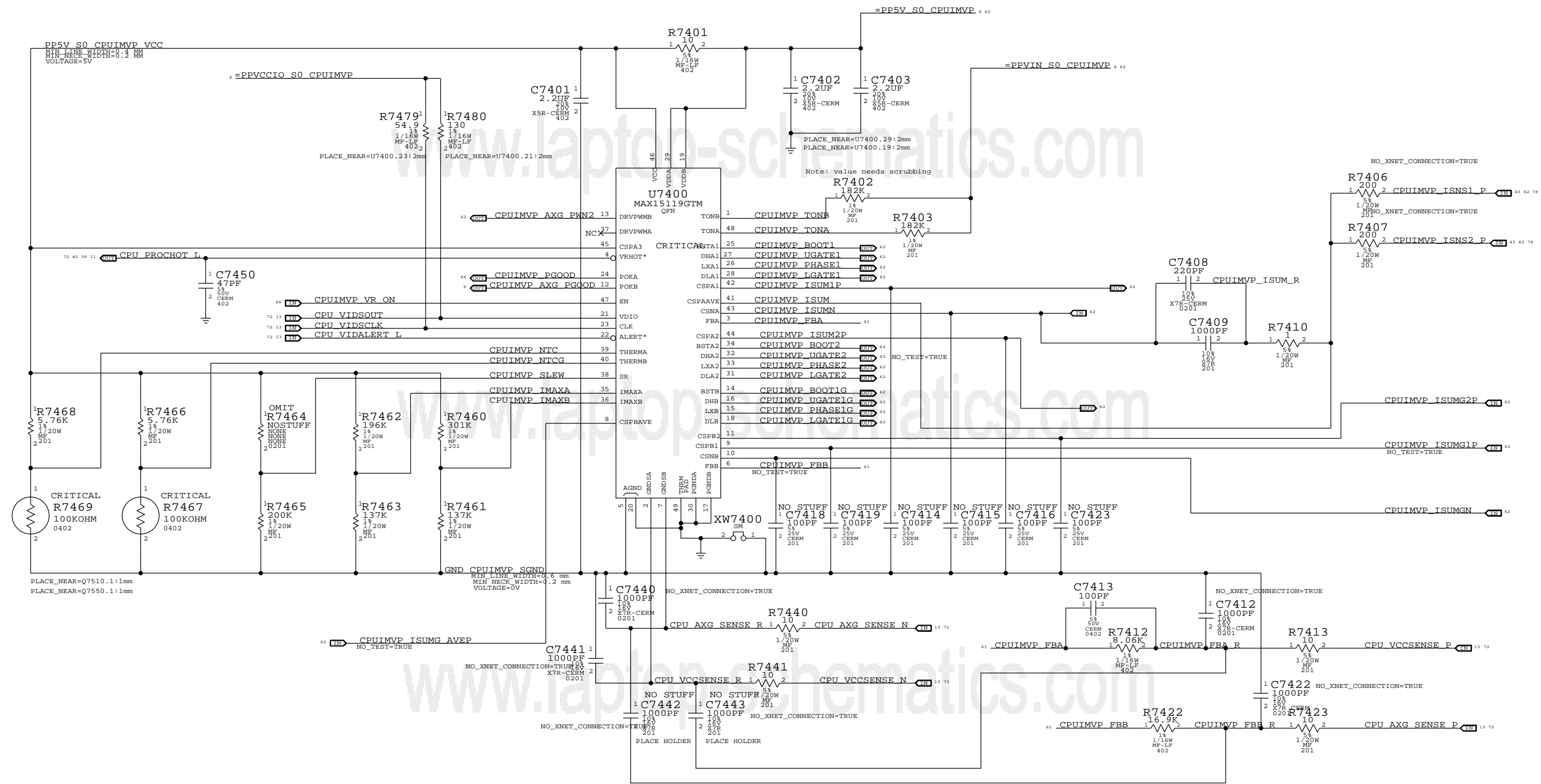
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138S0812	1	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7121	CRITICAL	




SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
System Agent Supply			
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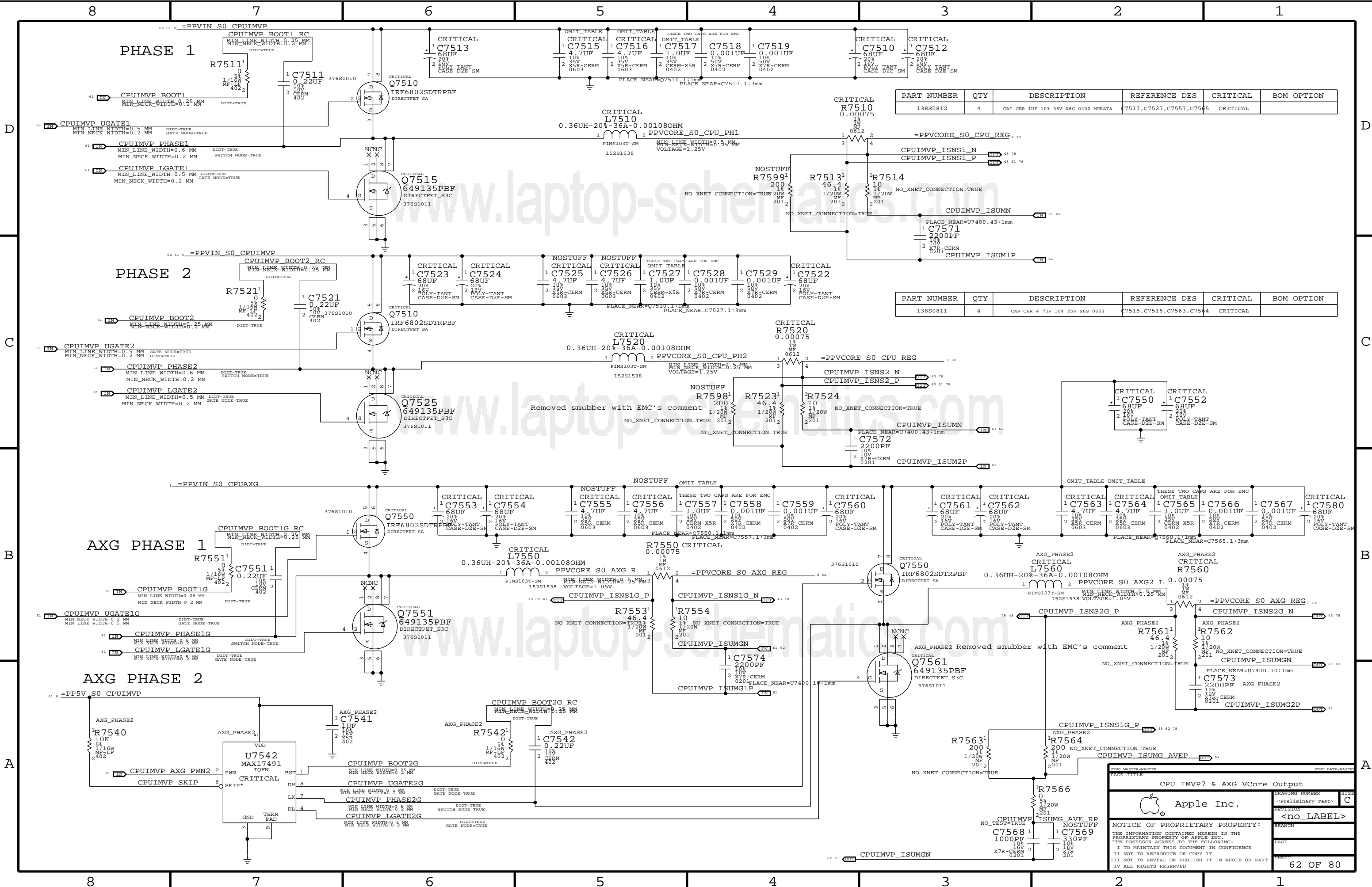
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SYMC MASTER-MASTER		SYMC DATE-MASTER	
PAGE TITLE			
CPU IMVP7 & AXG VCore Regulator			
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SHEET		61 OF 80	

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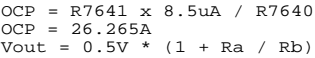
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	4	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7517,C7527,C7557,C7565	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP CER 4 7UF 10% 25V X6S 0603	C7515,C7516,C7563,C7564	CRITICAL	

PAGE TITLE		PAGE NUMBER	
CPU IMVP7 & AXG VCore Output		62 OF 80	
Apple Inc.		DRAWING NUMBER	SIZE
		<Preliminary Test>	C
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PART NUMBER	QTY	DE
138S0812	1	CAP CER 1UF

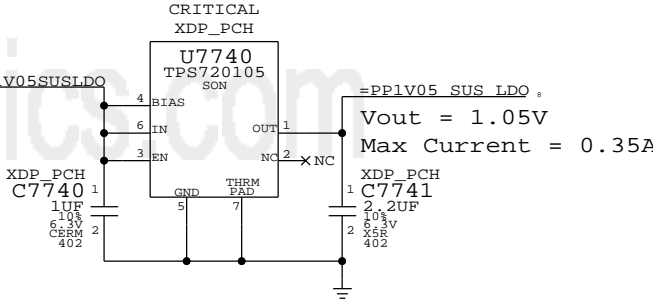
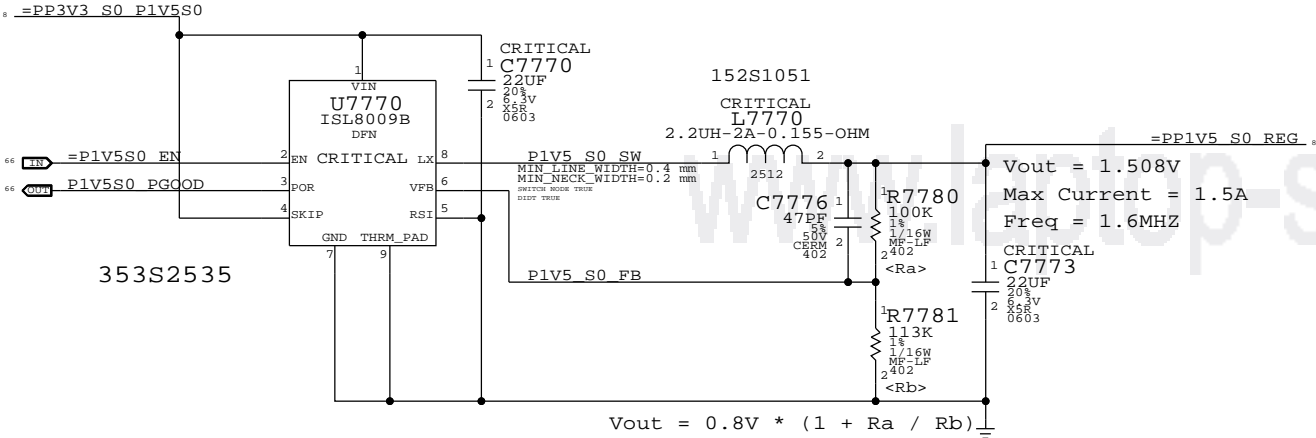
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138S0812	1	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7624	CRITICAL	



1.5V S0 Switcher

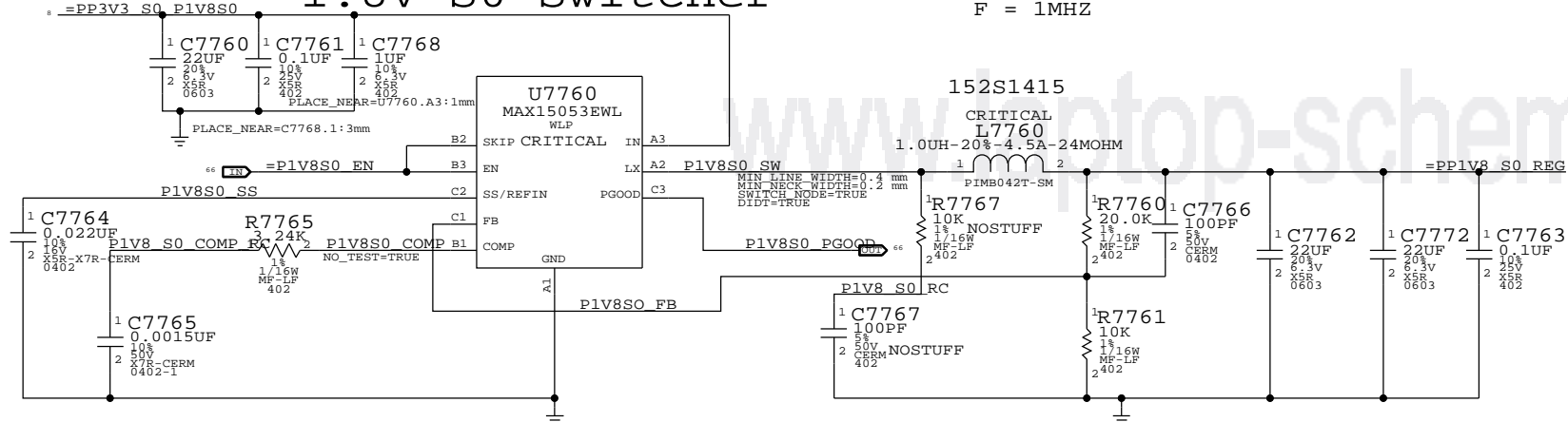
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



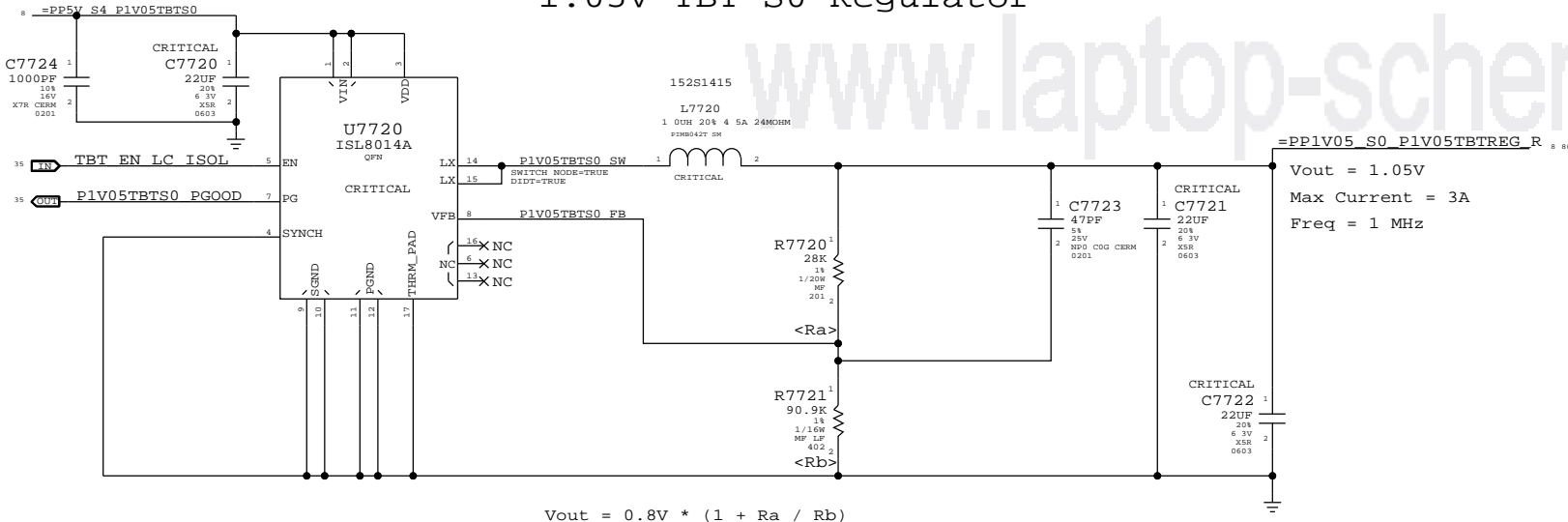
1.8V S0 Switcher

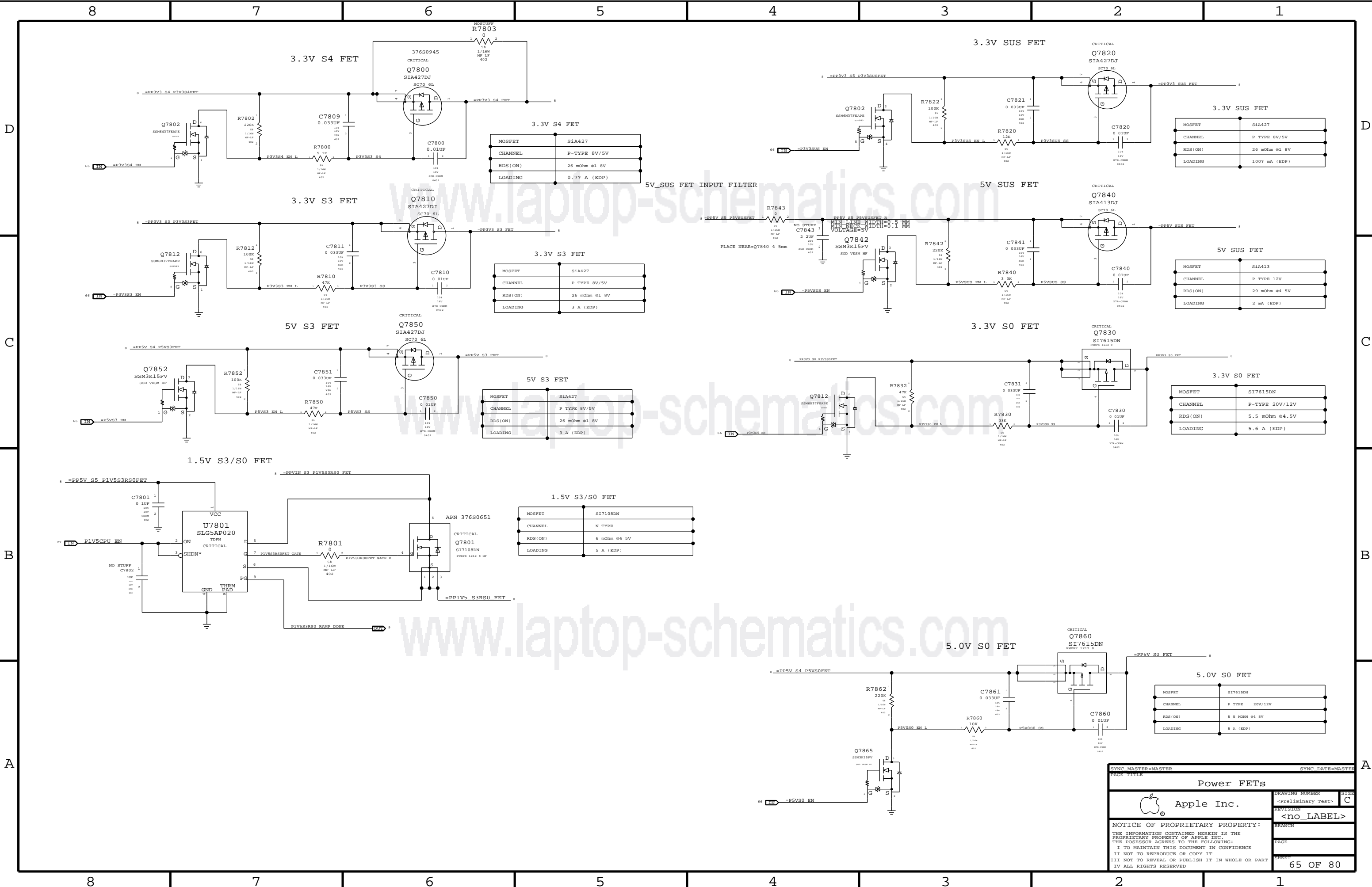
Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.05V TBT S0 Regulator

Vout = 1.05V
Max Current = 3A
Freq = 1 MHz





3.3V S4 FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

5V S3 FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V SUS FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

MOSFET	SIA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

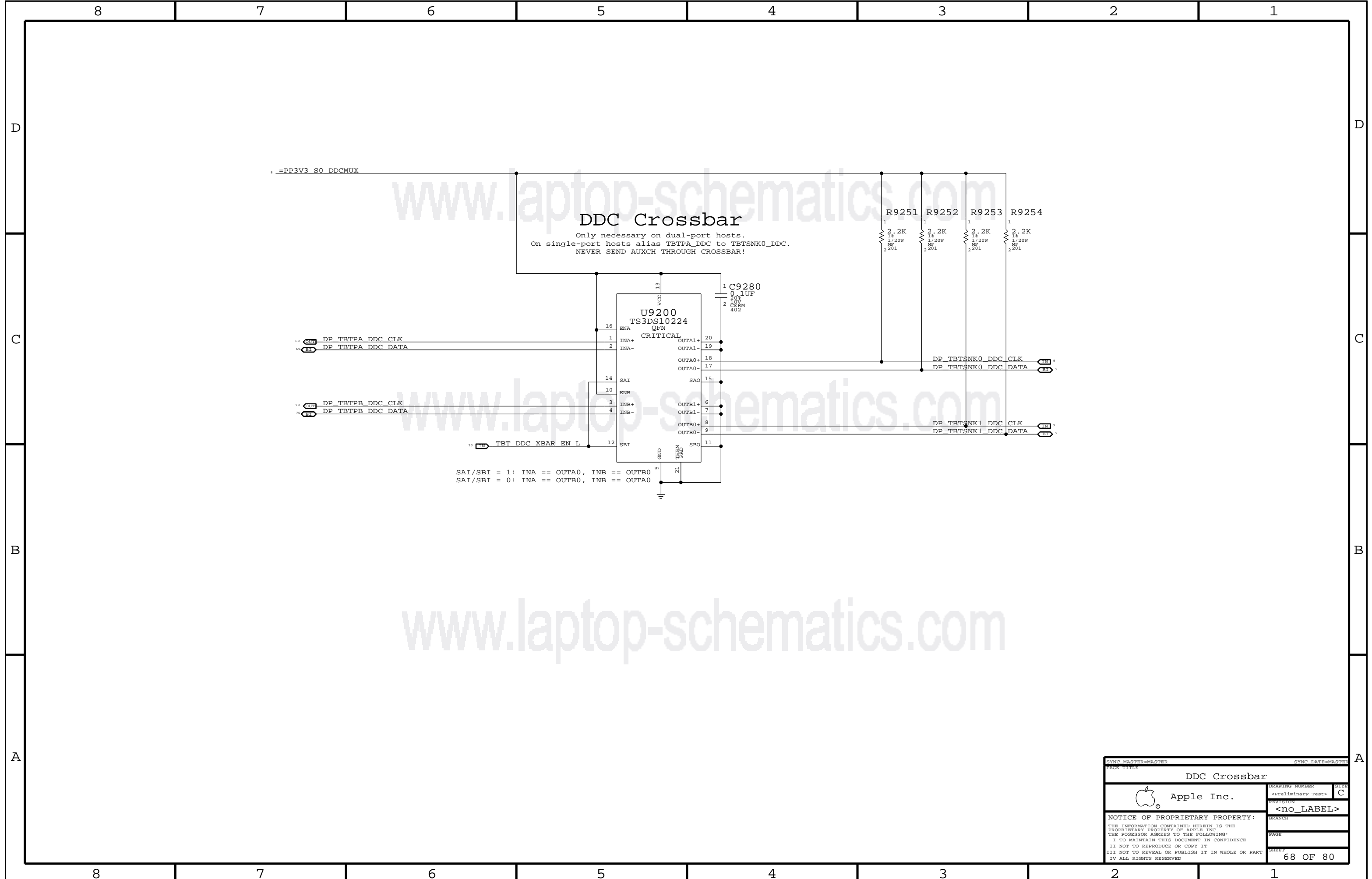
3.3V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Power FETs		DRAWING NUMBER	SIZE
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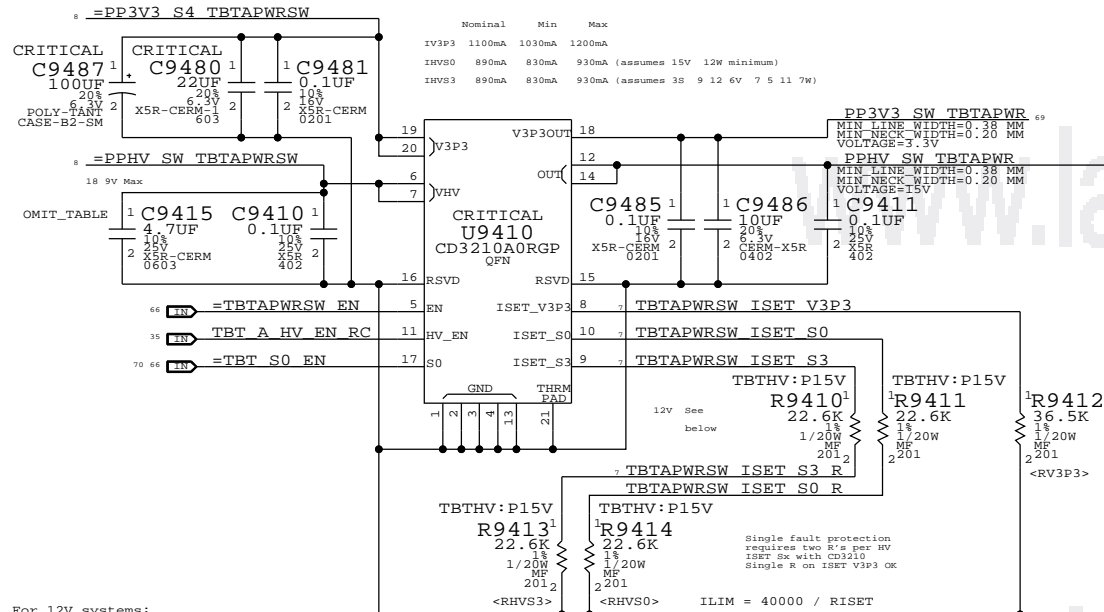


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP CER 4 7UF 10% 25V X5R 0603 MURATA	C9415	CRITICAL	

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices

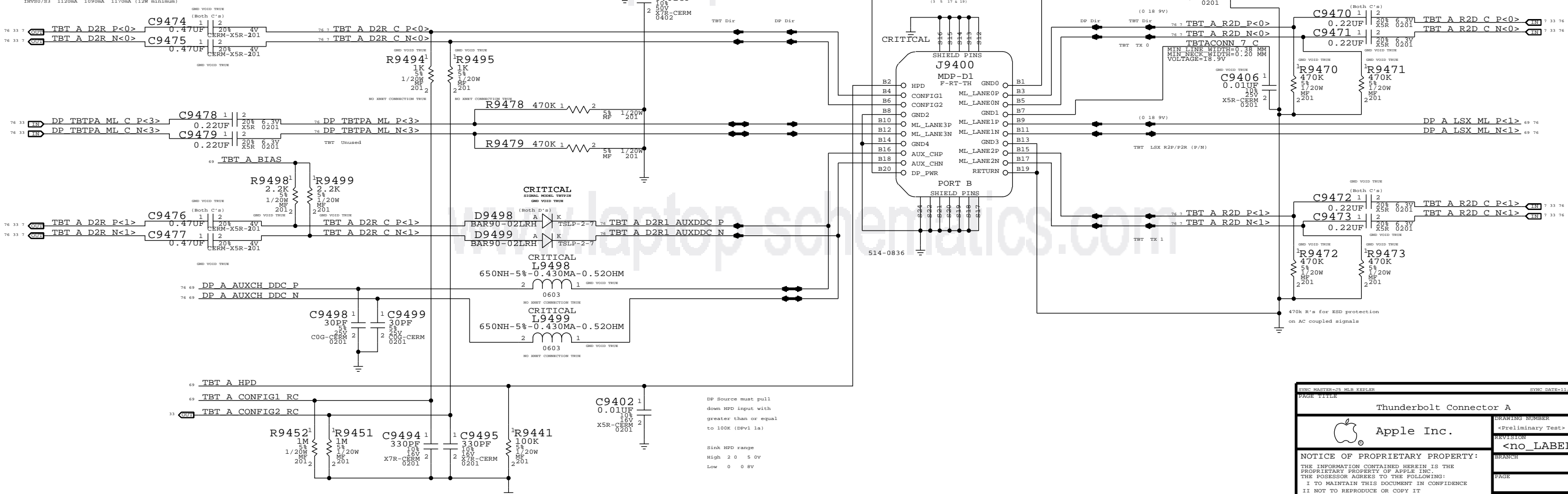
=PP3V3 S4 TBTAPWRSW



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

Nominal	Min	Max
---------	-----	-----

Nominal	Min	Max
00000000 - 00000000	00000000	007F0000



DP Source must pull
down HPD input with


greater than or equal

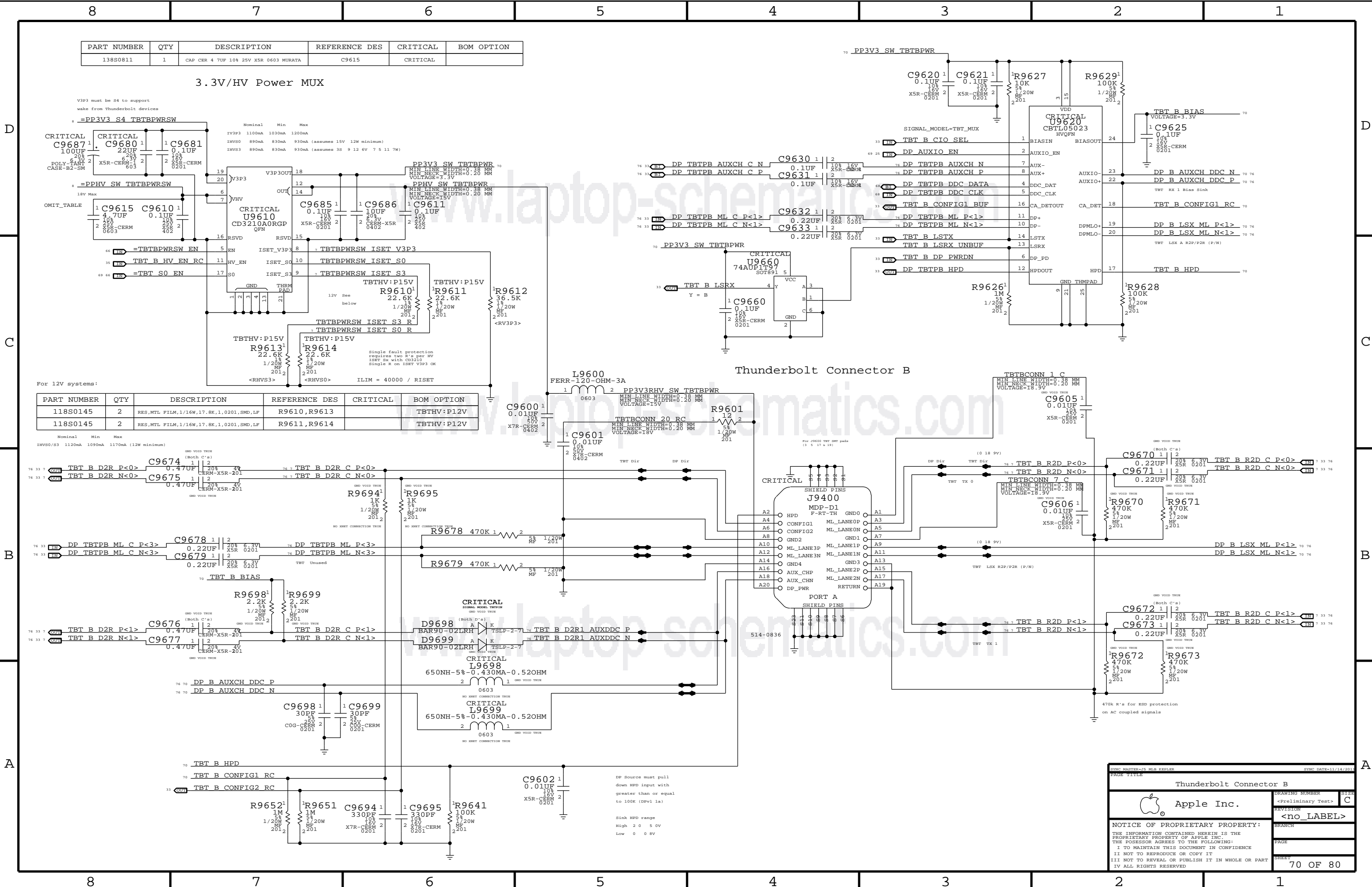
Sink HPD range

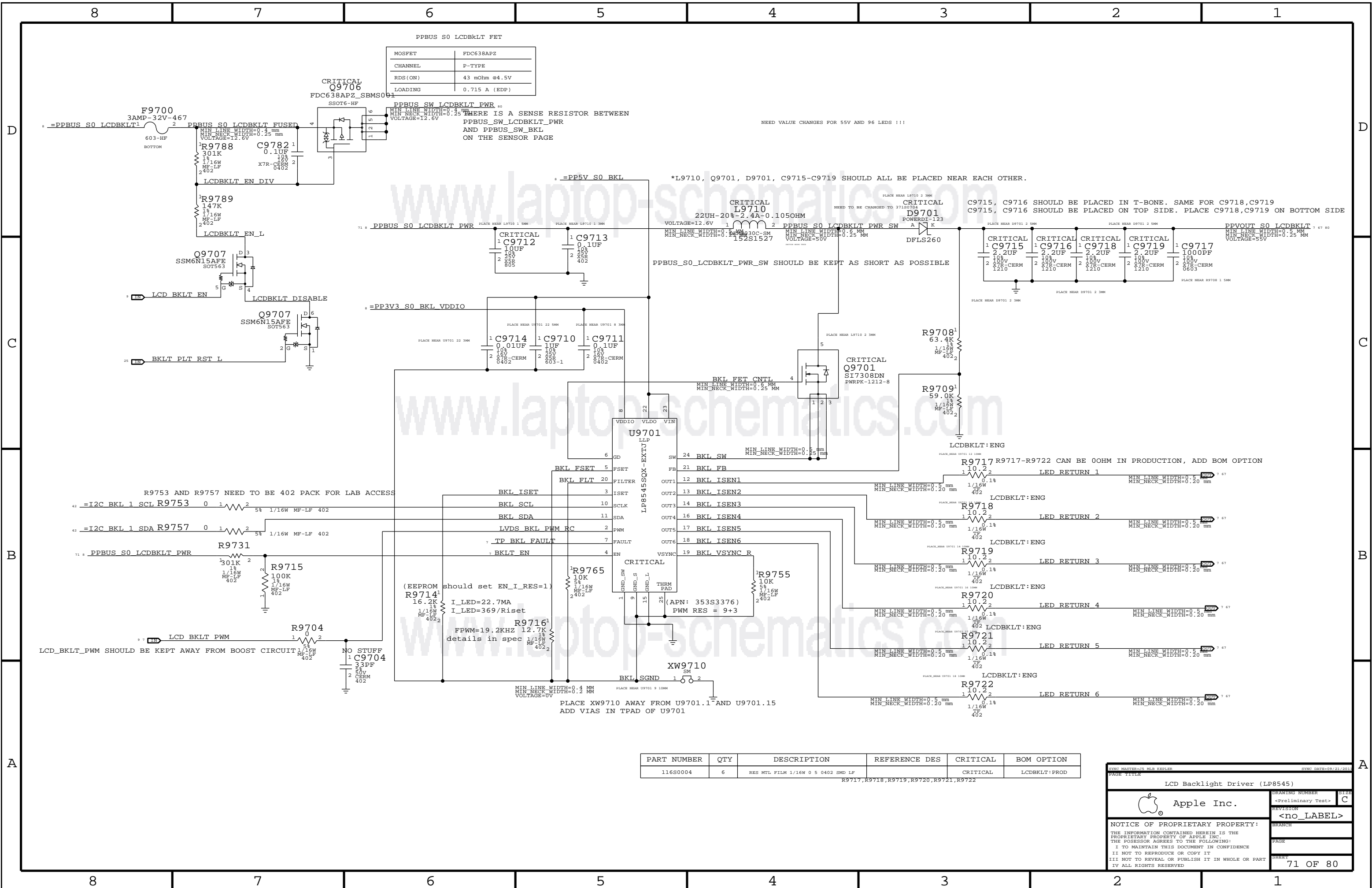
High 20 5.0V

High	2.5	5.0V
Low	0	0.8V

LOW 0 0 8V

SYNCH MASTER=05 NLS KEPLER		SYNCH DATE=11/14/2011	
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Thunderbolt Connector A			
		DRAWING NUMBER	
		<Preliminary Test>	
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		SHEET	
		69 OF 80	





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES MTL FILM 1/16W 0 5 0402 SMD LF	R9717,R9718,R9719,R9720,R9721,R9722	CRITICAL	LCDBKLT:PROD

SYNCHRONOUS MOS DRIVER		SYNCHRONOUS MOS DRIVER	
PAGE TITLE			
LCD Backlight Driver (LP8545)			
DRAWING NUMBER		SIZE	
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71 OF 80			

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
CLK LPC 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
HDA 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK SLOW	*	8 MIL	?

SPI Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 55G	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET TYPE		PHYSICAL		SPACING		
000	LPC_AD	LPC_50S	LPC	LPC_AD<3..0>				7 17 39 41
000	LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L				7 17 39 41
000	LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L				25
000	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R				19 25
000		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC				7 25 39
000		CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS				7 25 41
000	SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK				7 17 42
000	SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA				7 17 42
000	SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK				17 42
000	SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA				17 42
000	SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SML_PCH_1_CLK				17 42
000	SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SML_PCH_1_DATA				17 42
000	HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK				17 51
000		HDA_50S	HDA	HDA_BIT_CLK_R				17
000	HDA_SYNC	HDA_50S	HDA	HDA_SYNC				17 51
000		HDA_50S	HDA	HDA_SYNC_R				17
000	HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L				17
000		HDA_50S	HDA	HDA_RST_L				17 51
000	HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0				17 51
000		HDA_50S	HDA	AUD_SDI_R				51
000	HDA_SDOUIT	HDA_50S	HDA	HDA_SDOUIT				17 51
000		HDA_50S	HDA	HDA_SDOUIT_R				17 25
000	SPI_CLK	SPI_55S	SPI	SPI_CLK_R				17 41
000		SPI_55S	SPI	SPI_CLK				41
000	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R				17 41
000		SPI_55S	SPI	SPI_MOSI				41
000	SPI_MISO	SPI_55S	SPI	SPI_MISO				17 41
000	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L				17 41
000		SPI_55S	SPI	SPI_CS0_L				41
000	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P				7 17 36
000	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N				7 17 36
000	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P				7 17 36
000	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N				7 17 36
000	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P				7 36
000	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N				7 36
000	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P				7 17 36
000	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N				7 17 36
000	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P				7 17 36
000	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N				7 17 36
000	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P				7 36
000	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N				7 36
000	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P				7 36
000	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N				7 36
000	PCIE_CLK100M_BCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P				7 17
000	PCIE_CLK100M_BCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N				7 17
000	PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P				7 17 33
000	PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N				7 17 33
000	PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P				17
000	PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N				17
000	PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P				17
000	PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N				17
000		CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK				17
000		CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN				7 17 25
000	PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P				7 9 17
000	PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N				7 9 17
000	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P				7 9 17
000	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N				7 9 17
000	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P				7 17 36
000	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N				7 17 36
000	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P				7 17 36
000	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N				7 17 36
000	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P				7 9 17
000	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N				7 9 17
000	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P				7 17
000	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N				7 17
000	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>				7 9 33
000	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>				7 9 33
000	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>				7 33
000	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>				7 33
000	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>				7 9 33
000	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>				7 9 33
000	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>				7 9 33
000	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>				7 33

8	7	6	5	4	3	2	1
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D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

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		SHEET	77 OF 80

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	= 2:1_SPACING	?
THERM	*	= 2:1_SPACING	?
AUDIO	*	= 2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1TO1_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1TO1_55S	*	SENSE_1TO1_55S
THERM_1TO1_55S	*	THERM_1TO1_55S
DIFFPAIR	*	DIFFPAIR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL CONSTRAINT_SET		NET TYPE		
		PHYSICAL	SPACING	
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPUTHMSNS D2 P 46
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPUTHMSNS D2 N 46
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPU THERMD P 9 10
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPU THERMD N 9 10
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GPUTHMSNS D P 46
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GPUTHMSNS D N 46
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GPU TDIODE P 46
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	GPU TDIODE N 46
4600	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	TBT THERMD P 46
4600	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	TBT THERMD N 46
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	DDR3THMSNS D1 P 46
	SENSE_DIFFPAIR	THERM_1T01_55S	THERM	DDR3THMSNS D1 N 46
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVCCIOS0 CS P 43 63
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVCCIOS0 CS N 43 63
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPU VDDQ SENSE P 13
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPU VDDQ SENSE N 13
4600	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCD PANEL P 43
4600	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCD PANEL N 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 1V35 S3 MEM P 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 1V35 S3 MEM N 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS SSD P 37 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS SSD N 37 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 3V3 S0 SSD R P 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 3V3 S0 SSD R N 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS WLAN P 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS WLAN N 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCDBKIT P 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCDBKIT N 43
4600	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS TBT P 80
4600	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS TBT N 80
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 1V35 S3 MEM R P 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS 1V35 S3 MEM R N 43
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	VCCSA50 CS P 58 80
	SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	VCCSA50 CS N 58 80
4635	HDMI_CLK	HDMI_90D	HDMI	HDMI IG CLK C P 7 9 36
4635	HDMI_CLK	HDMI_90D	HDMI	HDMI IG CLK C N 7 9 36
4635	HDMI_DATA	HDMI_90D	HDMI	HDMI IG DATA C P<2..0> 7 9 36
4635	HDMI_DATA	HDMI_90D	HDMI	HDMI IG DATA C N<2..0> 7 9 36

D1 Specific Net Properties


ELECTRICAL_CONSTRAINT_SET		NET TYPE			
		PHYSICAL	SPACING		
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 36
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 36
		1T01_DIFFEPAIR		CHGR_CSI_R_P	57
		1T01_DIFFEPAIR		CHGR_CSI_R_N	57
		1T01_DIFFEPAIR		CHGR_CSO_R_P	57
		1T01_DIFFEPAIR		CHGR_CSO_R_N	57
	USB_RT	USB_85D	USB	USB_BT_CONN_P	36
	USB_BT	USB_85D	USB	USB_BT_CONN_N	36
REF	USB_RT	USB_85D	USB	USB_BT_WAKE_P	36
REF	USB_RT	USB_85D	USB	USB_BT_WAKE_N	36
REF	AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 53 55
REF	AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 53 55
REF	AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 53 55
REF	AUDIO_DIFFEPAIR	DIFFEPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 53 55
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNSG_P	43
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNSG_N	43
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1G_P	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1G_N	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS2G_P	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS2G_N	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISUMG_R_P	43
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISUMG_R_N	43
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_OTHER_P	44
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_OTHER_N	44
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_COMPUTING_P	44
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_COMPUTING_N	44
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS_P	43
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS_N	43
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1_P	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS1_N	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS2_P	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISNS2_N	43 62
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISUM_R_P	43
REF	SENSE_DIFFEPAIR	SENSE_1T01_55S	SENSE	CPUIMVP_ISUM_R_N	43
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L01_L_P	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L01_L_N	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L01_R_P	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L01_R_N	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L02_L_P	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L02_L_N	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L02_R_P	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_L02_R_N	51 53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	51 54
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	51 54
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	RSUBIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	RSUBIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	LSUBIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	LSUBIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	HS_MIC_HI_RC	54
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	HS_MIC_LO_RC	54
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	HS_MIC_HI	54
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	HS_MIC_LO	54
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
REF	AUDIO_DIFFEPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
REF	USB_TP4D	USB_85D	USB	USB_TP4D_R_P	26 47
REF	USB_TP4D	USB_85D	USB	USB_TP4D_R_N	26 47
REF	USB_HUB	USB_85D	USB	PU_USBHUB_DN4_P	9
REF	USB_HUB	USB_85D	USB	PU_USBHUB_DN4_N	9
			SR_POWER	PP3V3_S5	7 8
			SR_POWER	PP3V3_S0	7 8
			SR_POWER	PPIV5_S3RS0_CPUDDR	8
			GND	GND	

DDR3 Loaded Segment Constraint Relaxations
Alternate single ended and differential impedances between devices.

Graphics ,SATA Constraint Relaxations
Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

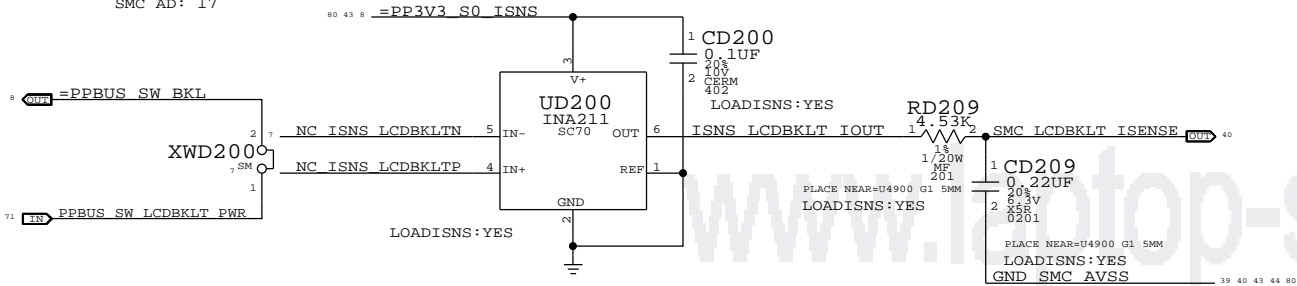
Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

SYNC MASTER-J5 MLB		SYNC DATE=07/29/2011	
PAGE TITLE			
Project Specific Constraints			
 Apple Inc.		DRAWING NUMBER <Preliminary Test>	
		SIZE C	
		REVISION <no_LABEL>	
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		78 OF 80	

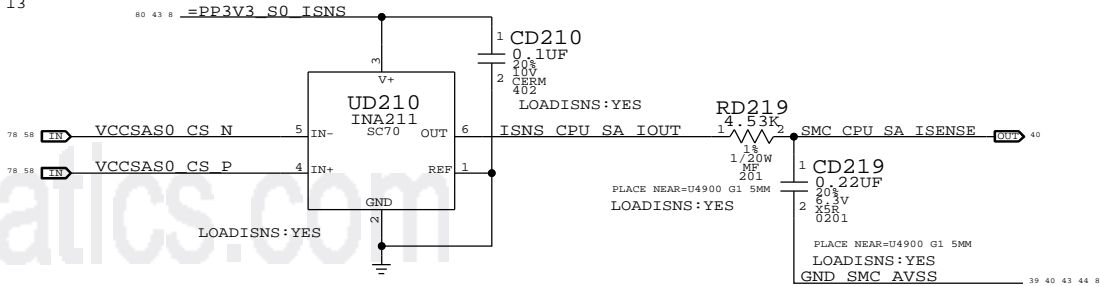
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
Rsense: 0.005 (RD200 / XWD200)
V across Rsense: 4.5 mV
SMC AD: 17



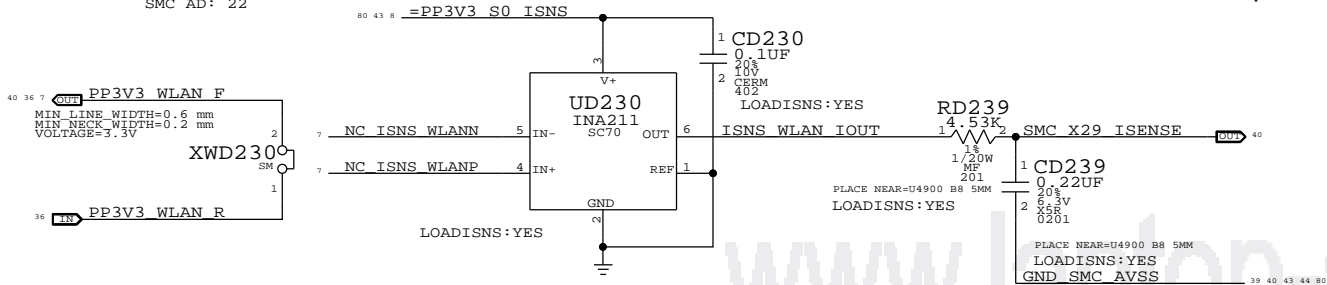
CPU SA Current Sense (IC2C)

Gain: 500x. EDP: 6 A
Rsense: 0.001 (R7140)
V across Rsense: 6 mV
SMC AD: 13



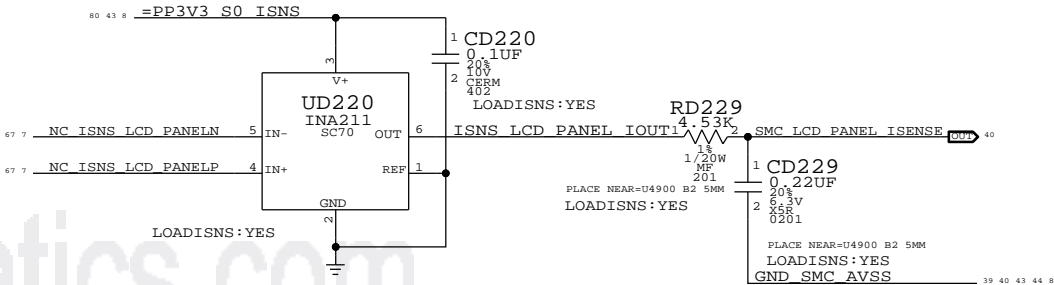
Airport X29 Current Sense (IAPC)

Gain: 500x. EDP: 1.06 A
Rsense: 0.005 (RD230 / XWD230)
V across Rsense: 5.3 mV
SMC AD: 22



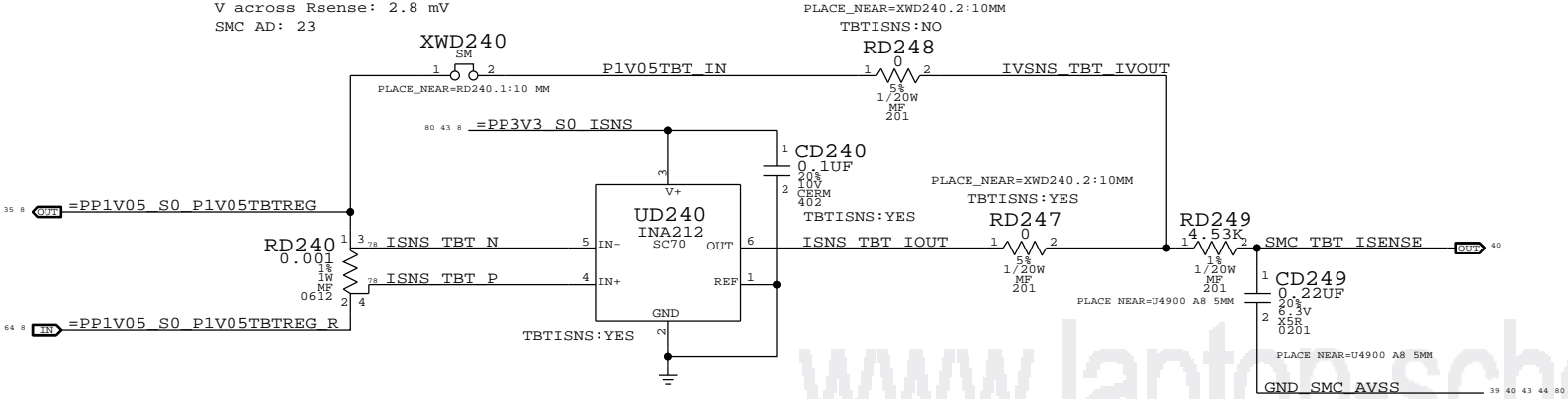
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R9020, XW9020)
V across Rsense: 5 mV
SMC AD: 15



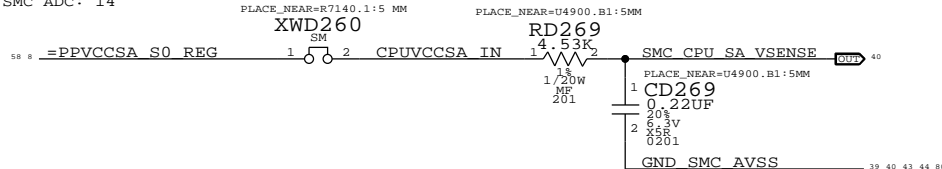
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
Rsense: 0.001 (RD240)
V across Rsense: 2.8 mV
SMC AD: 23



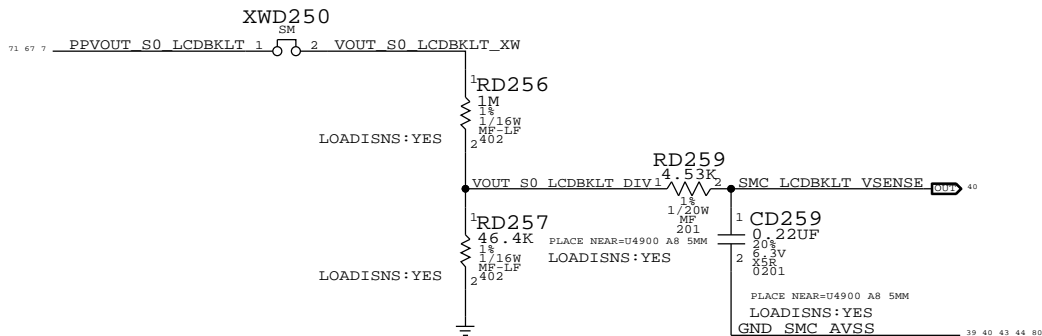
CPU SA Voltage Sense (VC2C)

Gain: 1x
SMC ADC: 14



LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

SYMC PARTS-CD SENSORS		SYMC DATE=07/11/2011	
PAGE TITLE			
Power Sensors: Extended		DRAWING NUMBER	SIZE
Apple Inc.		REVISION	C
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